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Ultra-fast Alternating Current Potential Drop Measurement System for Materials Characterization and Precision Impedance Analyzer for Eddy Current Measurement

Yuan Ji
Iowa State University

Ultra-fast alternating current potential drop measurement system for materials characterization and precision impedance analyzer for eddy current measurement

by

Yuan Ji

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John Bowler, Major Professor
Nicola Bowler
Degang Chen
Nathan Neihart
Jiming Song

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DEDICATION

I would like to dedicate this thesis to my wife Chun without whose support and encouragement I would not have been able to complete this work. I would also like to thank my family and friends for their loving guidance and financial assistance during the writing of this work.

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ABSTRACT

The alternating current potential drop method (ACPD) with four-point probe injects alternating current into the sample under test from the two outer drive pins and measures the voltage (potential) drop between the two inner pick-pins. This method can be used to measure electrical conductivity, linear permeability, coating depth, as well as crack size. However, the measurement speed and accuracy of present ACPD system need to be dramatically improved.

This work discusses the design, implementation and test of a novel ultra-fast standalone ACPD system. New and powerful hardware including high current transconductance amplifier and low noise amplifier provide a sound foundation for nearly perfect system level noise performance; new time domain to frequency domain conversion method increases the measurement speed without sacrificing noise performance. A general purpose calibration method is introduced so that the accuracy of this system is guaranteed.

With the development and introduction of this new ACPD instrument, ACPD method has evolved from a laboratory NDE method to a full blown technique that is ready for real world application.

The last chapter of this thesis discusses a simple but powerful lock-in amplifier based precision impedance analyzer. This impedance analyzer provides an economical solution to eddy current testing that requires highest precision.

CHAPTER 1. INTRODUCTION TO ALTERNATING CURRENT POTENTIAL DROP MEASUREMENT

1.1 Alternating Current Potential Drop Method

The alternating current potential drop method (ACPD) with four-point probe injects alternating current into the sample under test from the two outer drive pins and measures the voltage (potential) drop between the two inner pick-pins, as shown in Figure 1.1.

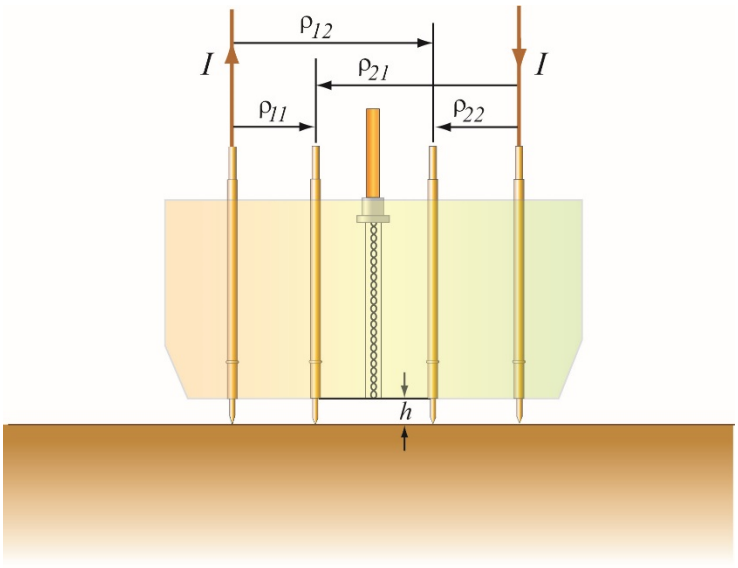


Figure 1.1 Alternating current I is injected into and extracted from the two outer drive pins. Potential drop is the measured voltage difference between the two inner pick-up pins.

For commonly used frequency of 1 Hz to 10 kHz, the normalized measured potential drop can be of the order of 10 microvolts or less. Thus four-point probe must be used in this method, rather than two point probe which introduces excessive uncertainty due to contact resistance. Similarly, alternating current is preferred over direct current, because of the undesired temperature sensitivity from thermocouple effect formed by the probe pins and the sample under test which is usually made from a different metal. However, alternating current will yield inductive pick-up effect which

is directly proportional to h in Figure 1.1. Minimizing h in ACPD measurement is important, since it reduces the inductive pick-up contribution to the measured signal.

The ACPD method requires good electrical contact with test piece and the four contact points are usually configured in a collinear fashion, forming a straight line. It is also a common practice to distribute the four pins horizontally with equal separation, or $\rho_{11} = \rho_{22} = \rho_{12} - \rho_{11}$ in Figure 1.1.

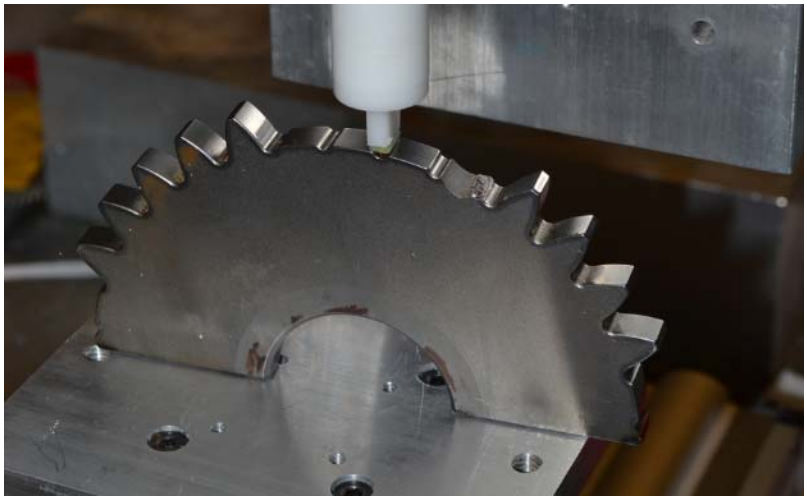


Figure 1.2 ACPD measurement using MK-2 probe on helicopter gears

It has been shown that ACPD measurements can be used to obtain electrical conductivity σ and linear permeability μ of sample under test [1, 2]. From measurement data of the frequencies below quasi-dc limit, conductivity σ can be obtained independent of sample permeability μ. Conversely, the sample permeability μ can be inferred from higher frequency measurement data, given already known conductivity σ. This distinctive advantage allows ACPD method to accurately characterize material conductivity σ and permeability μ, even if the material is ferrous, which is inaccurate for eddy current measurements due to its limited sensitivity at low frequency. In fact, the application of ACPD method is much more versatile than mere conductivity σ and permeability μ measurement. It has been shown that ACPD method can also be used to characterize plate

thickness [3], coating thickness [4], crack depth [5] and case hardening, all of which are achieved by interpretation of measurement data with assistance of theoretical models.

This chapter briefly discusses the theory of ACPD measurement, as well as the working principal and set-up of a typical distributed laboratory ACPD measurement system. Due to its fundamental limitations, distributed ACPD system consisting of commercial off the shelf instruments lack the performance and measurement speed to make ACPD a viable technology in the real world application. To improve the data quality and measurement speed of ACPD instrument, a different approach must be used. With the help of improved digital signal processing algorithm, integrating function blocks of ACPD measurement system into a single board yields improved signal to noise ratio of measured data at a fraction of time penalty compared with distributed laboratory ACPD measurement system. This dissertation covers the design, test and application of such instrument.

1.2 Alternating Current Potential Drop Theory

The theory of ACPD, which has been well established, is summarized in this section. In general, the ACPD from a four-point probe can be expressed as

$$V = \frac{I}{2\pi\sigma}[F(\rho_{22}) - F(\rho_{21}) - F(\rho_{12}) + F(\rho_{11})]\,, \qquad (1.1)$$

in which $F(\rho_{ij})$ can have different forms depending on the sample under test and frequency range. I is the current amplitude and ρ_{ij} denotes the distance from current inject point P_i to voltage pick-up points Q_i illustrated in Figure 1.4 for an arbitrary distribution of contact points.

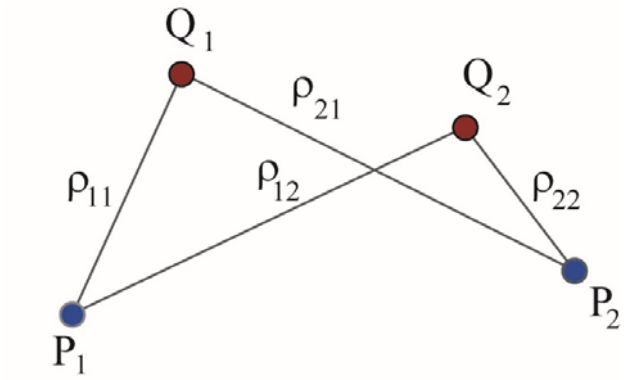


Figure 1.3 Planar illustration of four-point probe pin configuration

For a special case where frequency is zero (DC), and the test piece is a uniform half-space, then

$$F_{hs}(\rho) = \frac{1}{\rho} \tag{1.2}$$

For frequency higher than zero, if the test piece is homogeneous half-space metal, the $F_k(\rho)$ can be expressed as [6]

$$F_{hs}(\rho) = \frac{e^{ik\rho}}{\rho} + ik[E_1(-ik\rho) + \ln\rho], \tag{1.3}$$

where $k^2 = \mathrm{i}\omega\mu\sigma$, and $E_1(z)$ is exponential integral function. Please also note that when $k \to 0$, equation (1.3) reduces to (1.2)

For a finite thickness plate, there are two representations of the $F_k(\rho_{ij})$ functions depending on the thickness of the plate. If the plate with thickness T is somewhat thicker than 0.75 times the total pin span of an equally spaced four-point probe, then [7]

$$F_p(\rho) \approx -\mathrm{ik}\coth(\mathrm{ikT})\ln\rho +$$

$$\sum_n \left(\frac{\exp[\mathrm{ik}\sqrt{\rho^2+(2\mathrm{nT})^2}]}{\sqrt{\rho^2+(2\mathrm{nT})}} + \mathrm{ike}^{2\mathrm{iknT}} E_1\{-\mathrm{ik}[\sqrt{\rho^2+(2\mathrm{nT})} - 2\mathrm{nT}]\}\right) \tag{1.4}$$

If the plate is somewhat thinner than 0.75 times the total pin span of an equally spaced four-point probes, then [7]

$$F_p(\rho) \approx -\mathrm{ik}\coth(\mathrm{ikT})\ln\rho + \frac{2}{T}\sum_{\nu=1}^{\infty}\left(\frac{(\pi\nu)^2}{(\pi\nu)^2-(\mathrm{kT})^2} \times K_0\left[\frac{\rho}{T}\sqrt{(\pi\nu)^2-(\mathrm{kT})^2}\right]\right) \quad (1.5)$$

where $K_0(z)$ is zero order modified Bessel function of the second kind. If the plate is thinner than the four point probe pin separation, then [7] the approximation

$$F_{tp}(\rho) \approx -\mathrm{ik}\coth(\mathrm{ikT})\ln\rho \quad (1.6)$$

is valid.

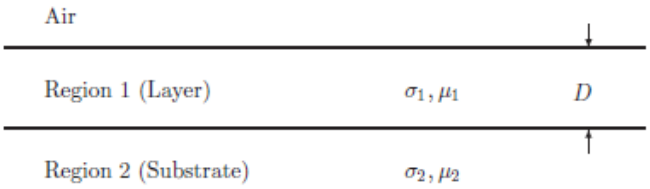


Figure 1.4 Cross-section view of a coated half-space conductor

For a coated half-space conductor with coating thickness of D, as illustrated in Figure 1.4, then [8]

$$F_c(\rho) = F_{hs,1}(\rho) + F_{layer}(\rho) \quad (1.7)$$

The first term in expression (1.7) denotes expression (1.3) in region 1 of Figure 1.4. The second term in expression (1.7) can be expressed as [8]

$$F_{\text{layer}}(\rho) = -2\int_0^{\infty}\frac{\gamma_1}{\kappa}\left[\frac{\Gamma e^{-2\gamma_1 D}}{1+\Gamma e^{-2\gamma_1 D}}J_0(\kappa\rho)\right]d\kappa \quad (1.8)$$

where,

$$\Gamma = \frac{\gamma_1/\sigma_1-\gamma_2/\sigma_2}{\gamma_1/\sigma_1+\gamma_2/\sigma_2}, with\ \gamma_i = \sqrt{\kappa^2 - \mathrm{i}\omega\mu_i\sigma_i} \quad (1.9)$$

$J_0(z)$ is the zero order Bessel function of the first kind.

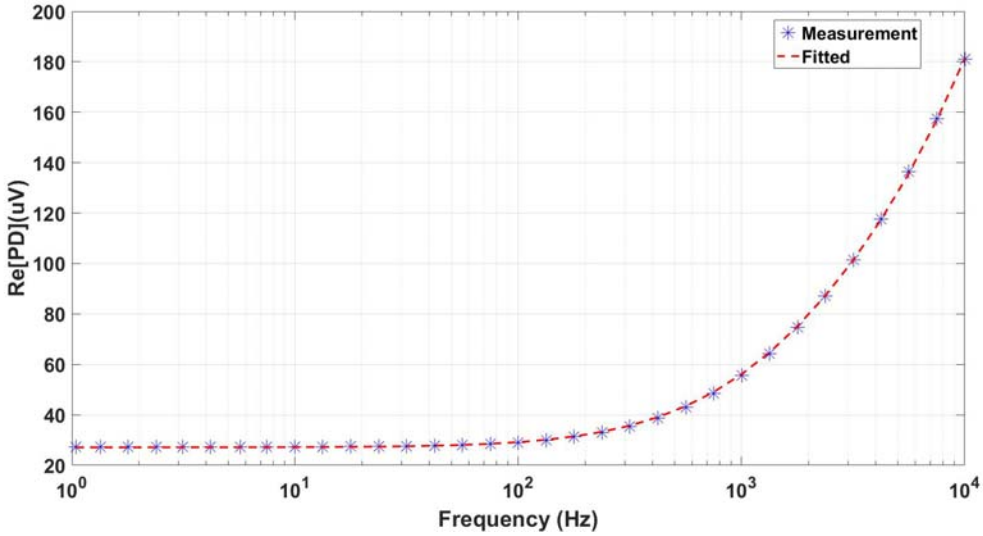
As mentioned in previous section, the alternating drive current will give rise to an undesired inductive pick-up voltage that can be expressed as [1]

$$\epsilon = \frac{I}{2\pi\sigma}[F_\epsilon(\rho_{22}) - F_\epsilon(\rho_{21}) - F_\epsilon(\rho_{12}) + F_\epsilon(\rho_{11})], \tag{1.10}$$

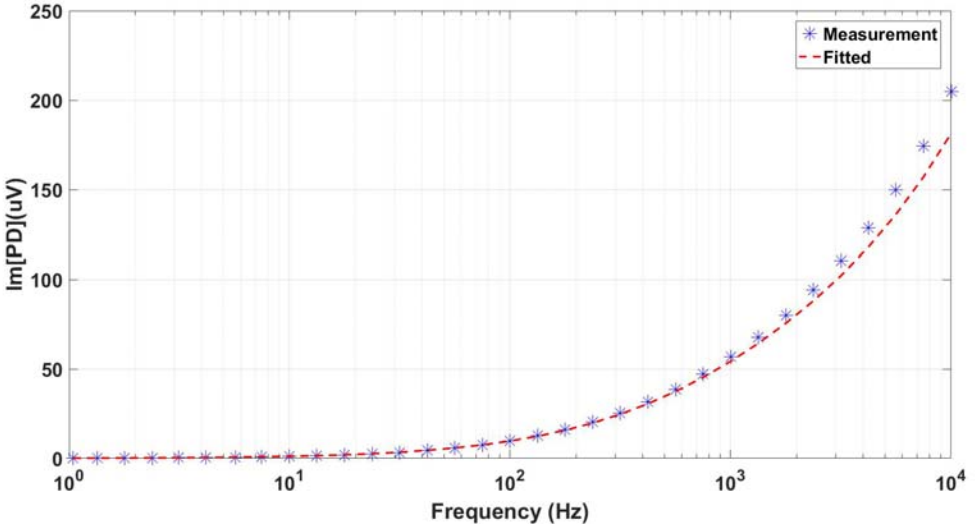
where

$$F_\epsilon(\rho) = \frac{h}{\mu_r}k^2 \ln\rho, \tag{1.11}$$

and μ_r is the relative permeability of the sample under test.



(a)



(b)

Figure 1.5 ACPD measurement result for (a) real part of potential drop and (b) imaginary part of potential drop

The data in Figure 1.5 is acquired on specimen 8055 using a 1.5 mm pin separation probe. Please note the difference between theory and measurement in the imaginary part of the potential drop, which is an example of inductive pick-up described in expressions (1.10) and (1.11).

The difference can be expressed as

$$\Delta V = j\omega L_{12} I, \tag{1.12}$$

where L_{12} is the mutual induction in the pick-up circuit due to the drive current and by estimating L_{12}, a correction to the data can be carried out.

1.3 Alternating Current Potential Drop Measurement System

Essentially, the result of ACPD measurement is the trans-impedance calculated from the pick-up pin voltage and drive current. However, the value of this trans-impedance is quite small compared with the normal input range of an impedance analyzer or LCR meter. To suite the needs of ACPD measurements in the lab, a custom designed measurement system is built using commercially available instruments and components, shown in Figure 1.6. The heart of this setup is a Stanford Research Systems SR830 DSP lock-in amplifier which has a frequency range of 1 mHz to 102 kHz. The lock-in amplifier (LIA) is normally used to detect and measure weak signal as small as a few nanovolt, even when the useful signal is dominated by much larger noise signal. Figure 1.7 [9] shows a simplified block diagram of a typical analog LIA.

The simplest case is that both signal input and reference signal are sinuous waves of the same frequency, then we have

$$V_{sa} = V_s \cos(\omega_0 t + \theta) \tag{1.12}$$

$$V_{vco} = V_r \cos(\omega_0 t) \tag{1.13}$$

where θ is the phase difference between those two signals.

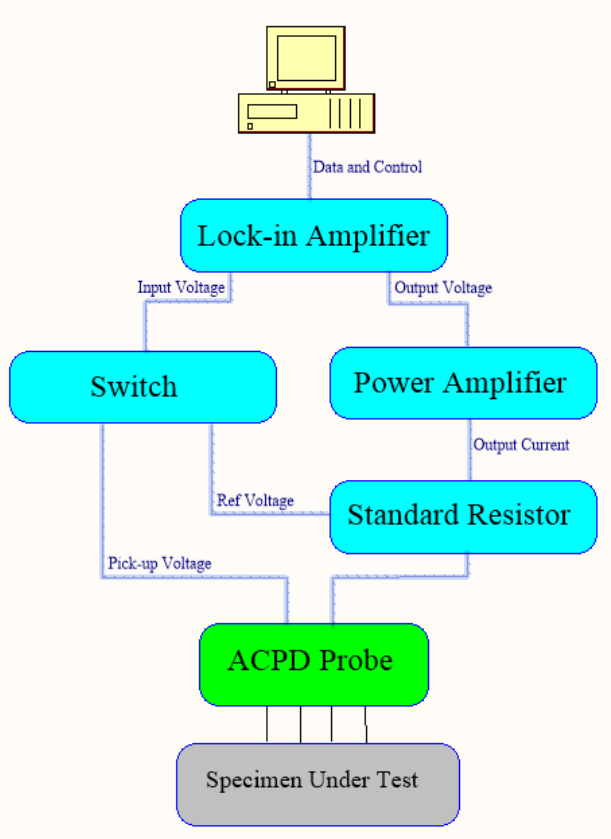


Figure 1.6 Block diagram of ACPD measurement system

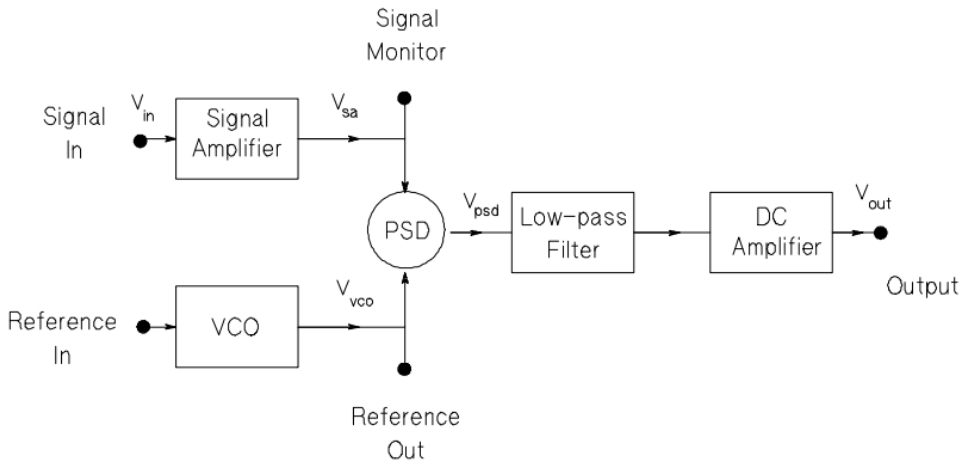


Figure 1.7 Diagram of an analog LIA including a voltage controlled oscillator(VCO) and a phase sensitive detector(PSD)

Phase sensitive detector (PSD) can be treated as an analog multiplier in this case, then

$$V_{\text{psd}} = V_{\text{sa}}V_{\text{vco}} = V_s\cos(\omega_0 t + \theta)V_r\cos(\omega_0 t) = \frac{1}{2}V_sV_r\cos(\theta) + \frac{1}{2}V_sV_r\cos(2\omega_0 t + \theta) \quad (1.14)$$

After a low pass filter (LPF) following the PSD, the second term of (1.14) on the right is removed. Assuming the DC amplifier in Fig 1.7 has a gain of 2, then

$$V_{\text{out},0} = V_sV_r\cos(\theta) \quad (1.15)$$

If the reference input is shifted by $\frac{1}{2}\pi$, after the same procedure, we get

$$V_{\text{psd}} = V_{\text{sa}}V_{\text{vco}} = V_s\cos(\omega_0 t + \theta)V_r\cos(\omega_0 t + \frac{1}{2}\pi) = -V_s\cos(\omega_0 t + \theta)V_r\sin(\omega_0 t)$$

$$= \frac{1}{2}V_sV_r\sin(\theta) - \frac{1}{2}V_sV_r\sin(2\omega_0 t + \theta) \quad (1.16)$$

The second term of (1.16) on the right is removed by low pass filter, yielding

$$V_{\text{out},\frac{1}{2}\pi} = V_sV_r\sin(\theta) \quad (1.17)$$

Combine (1.15) and (1.17), we are able to retrieve the amplitude and phase of the input signal with respect to reference signal.

In case of noise signal $V_n\cos(\omega_n t)$, assume LPF being a first order RC low pass filter (LPF), we get

$$V_{\text{out}} = \frac{V_nV_r}{\sqrt{1+(\Delta\omega\text{RC})^2}}\cos[\Delta\omega t - \arctan(\Delta\omega\text{RC})]\,, \quad (1.18)$$

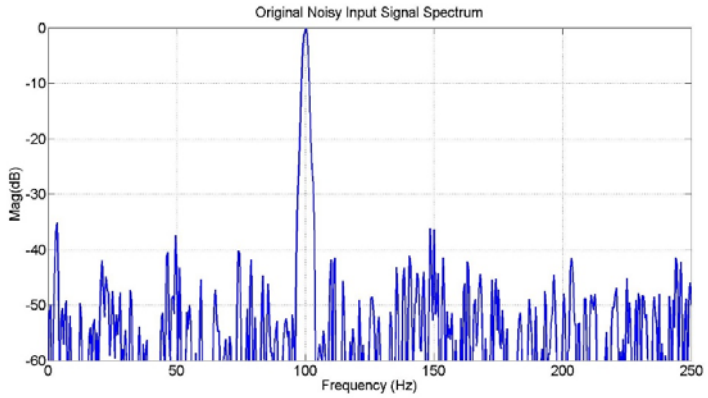
where $\Delta\omega = \omega_n - \omega_0$

In steady state, $\Delta\omega t \gg \arctan(\Delta\omega\text{RC})$, expression (1.18) can be simplified as

$$V_{\text{out}} = \frac{V_nV_r}{\sqrt{1+(\Delta\omega\text{RC})^2}}\cos(\Delta\omega t) \quad (1.19)$$

Expression (1.19) states that LIA's noise performance is directly related to the bandwidth of the LPF after PSD. The noise bandwidth of a first order RC LPF is $\frac{1}{4\text{RC}}$ (Hz), but note that the PSD is a double sideband(DSB) modulator, the actual noise bandwidth is $\frac{1}{2\text{RC}}$ (Hz). Increasing the RC

time constant of the LPF leads to enhanced noise performance of LIA. The PSD and LPF combination is equivalent to a bandpass filter centered at the frequency of interest. It is much easier to create a small bandwidth low pass filter than a small bandwidth (high Q) band pass filter. In modern DSP based LIA, the time constant can be as long as 30 seconds, making its equivalent noise bandwidth extremely small.



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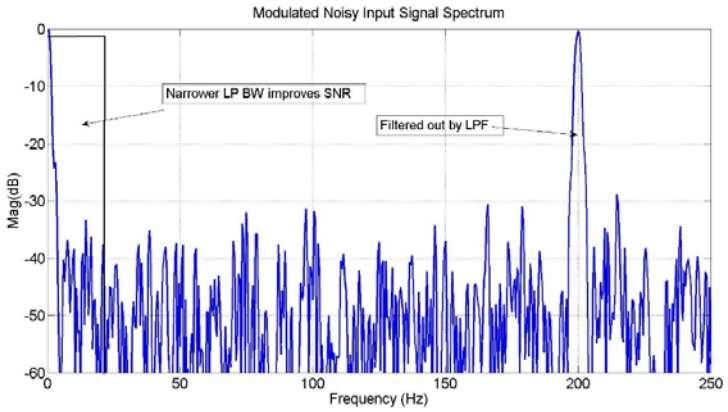


(b)

Figure 1.8 Spectrum of a noisy input signal before (a) and after (b) PSD

For a given input signal, narrower bandwidth LPF yields better signal to noise ratio, at the cost of measurement speed.

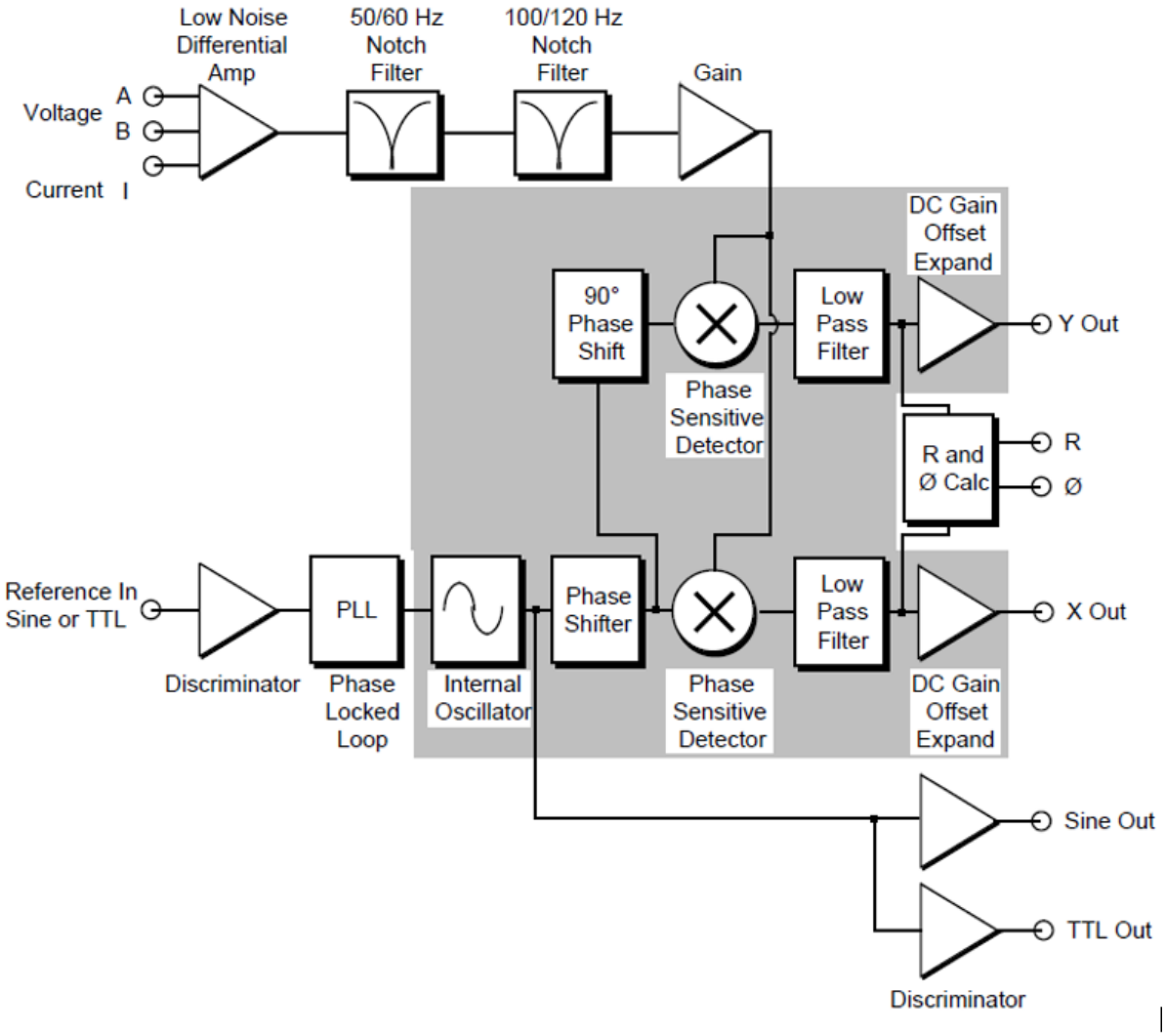


Figure 1.9 SR830 LIA functional block diagram

The actual function diagram shown in Figure 1.9 [10] is similar to the one in Figure 1.7. But operation and signal processing done by analog circuit in Figure 1.7 are handled by digital signal processor in Figure 1.9. Digital signal processing is superior to analog signal process in terms of harmonic rejection, output offsets, dynamic reserve and gain error [10].

In Figure 1.6, SR830 lock-in amplifier outputs a drive voltage signal to a Kepco bipolar operational power amplifier, model number BOP 20-20M. This power amplifier is configured into a transconductance amplifier which converts voltage input from LIA into a current output for the

four-point probe. Internally the voltage drive is the reference voltage in Figure 1.7. A current sampling resistor is in series with four-pint probe. The voltage across this resistor is linearly proportional to the drive current. The pick-up voltage from the probe normalized by this drive current is the end result of this test measurement. Since the SR830 LIA can only process one signal at one time, a DPDT mechanical relay mounted in the switch box is used to select which of the two signals is connect to the differential input of LIA.

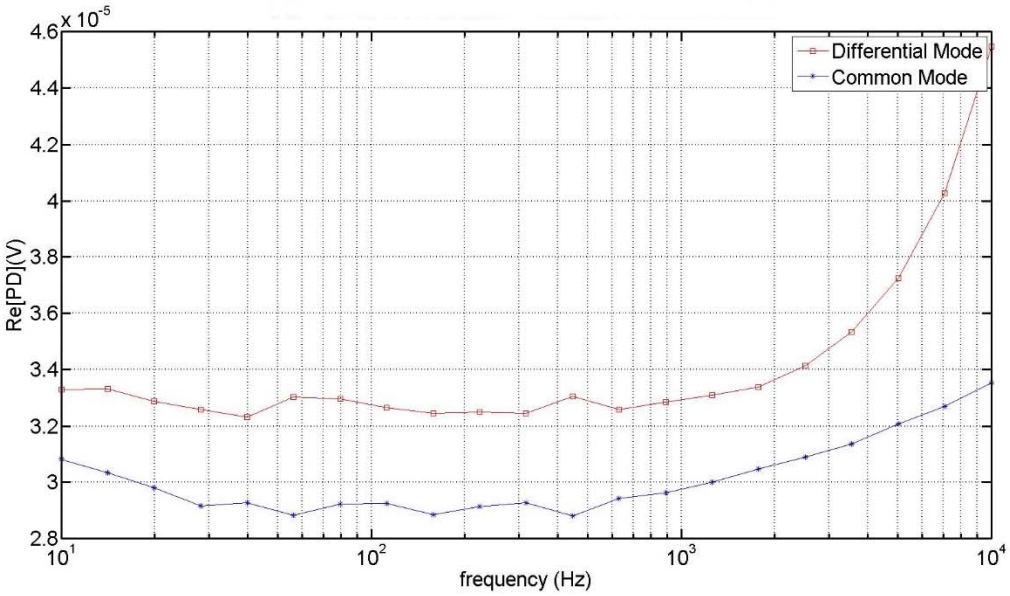


Figure 1.9 Comparing differential mode and common mode potential drop.

In reality, the small differential pick-up voltage is of interest. But the common mode voltage due to contact resistance of connectors and resistance of cables make it very difficult for the LIA input analog front end to completely reject the common mode signal. The common mode voltage can be as high as 500 mV in amplitude, while the differential pick-up voltage is within range of several micro volts in amplitude. Even for an instrumentation amplifier that has common mode rejection ratio (CMRR) of 120 dB, it is still not enough to give a CMR error free measurement result. Another DPDT relay is used to toggle the polarity of pick-up input voltage, eliminating CMR error in software by measuring the pick-up voltage twice. Figure 1.9

demonstrates that with SR830 LIA's CMRR of 100 dB [10], the CMR error is actually on par with desired pick-up signal.

A PC based software written in C# is used to control the LIA and Switch box. Final result is saved in a text file which is later imported into Matlab for further analysis.

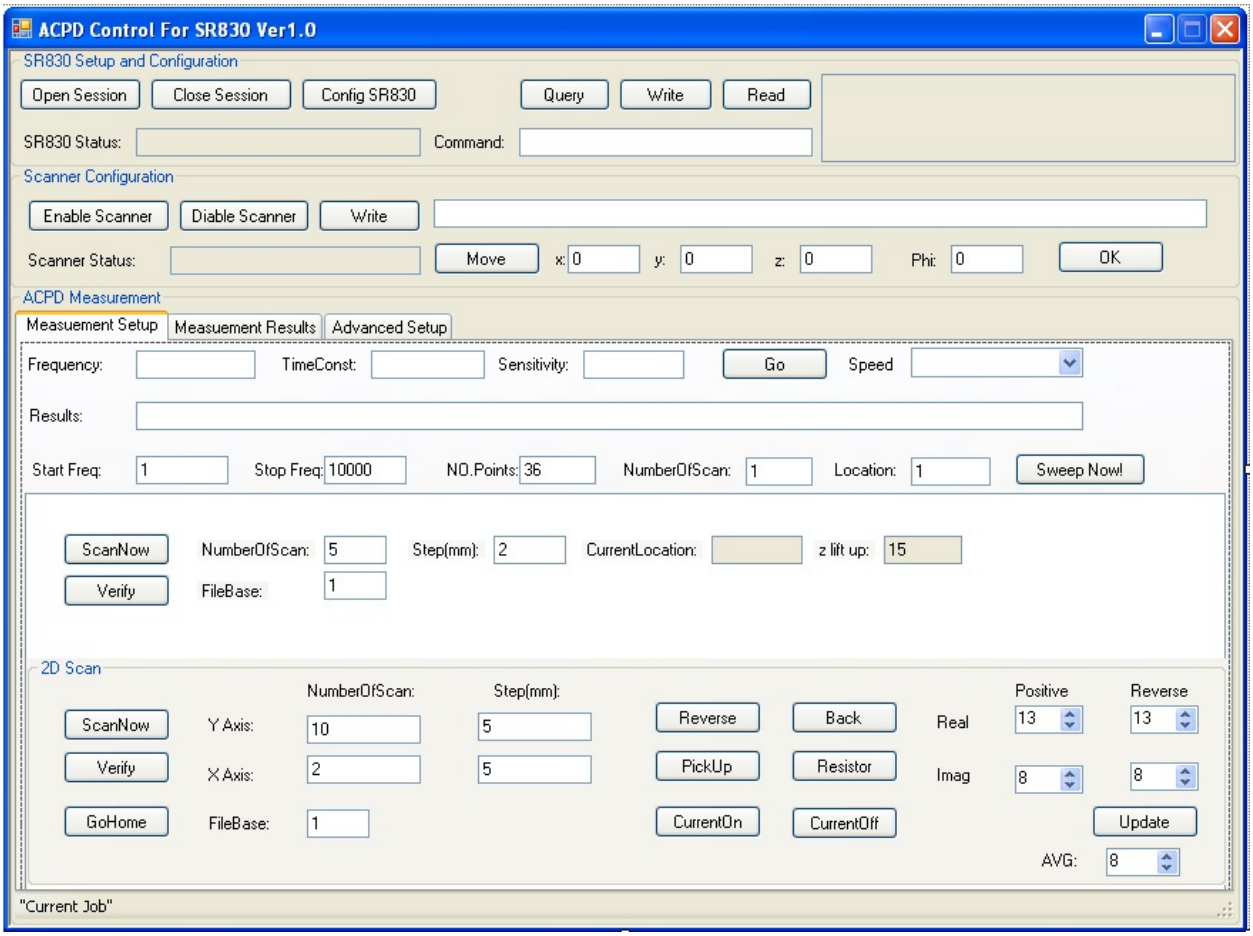


Figure 1.9 Software interface for ACPD measurement setup

1.4 Alternating Current Potential Drop Four-Point Probe Design

The four-point probe is the quintessential part of ACPD measurement system, which significantly affects the capability of this method.

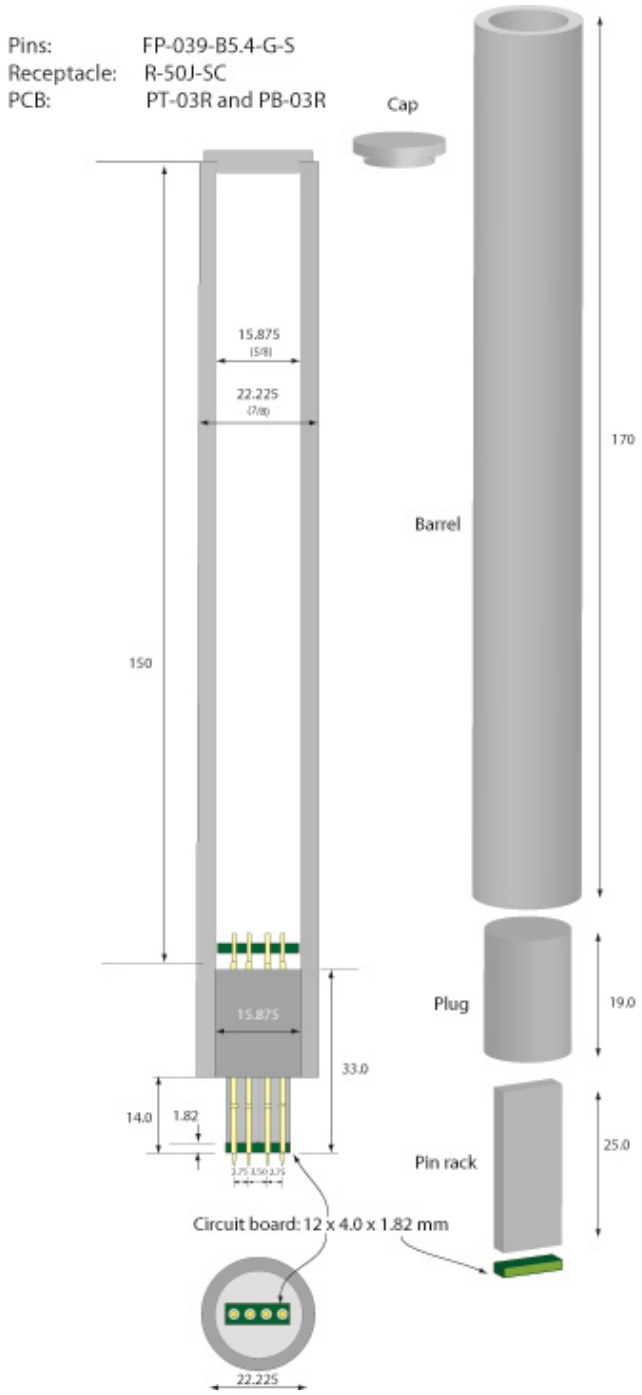


Figure 1.10 Design of MK-2 ACPD probe

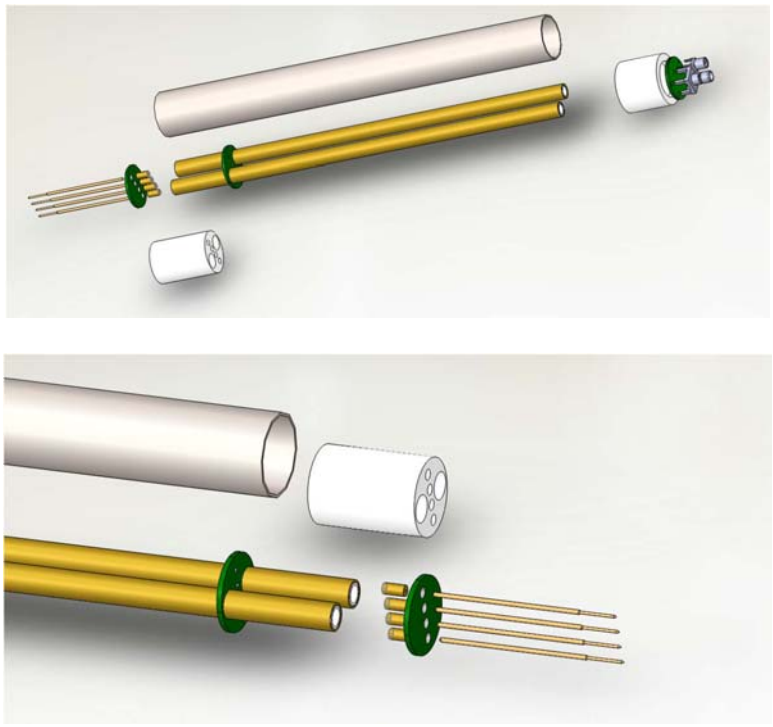


Figure 1.11 Design of MK-3 ACPD probe

MK-3 probe is a major upgrade from MK-2 probe. Precision bushes in MK-3 significantly reduces the measurement uncertainly associated with pin wiggling. Future ACPD probe will be integrated with active circuitry for better performance. Putting active circuitry such as instrumentation amplifiers and low pass filters within the probe increases system level signal to noise ratio, because amplified pick-up signal is less sensitive to external noise. Furthermore, if the transconductance amplifier is also integrated into the ACPD probe, mega hertz range ACPD measurement becomes possible.

1.5 Problem Statement

Section 1.3 discusses the ACPD measurement system composed of commercially available instruments. While providing data for ACPD experiments, this setup is not without its drawbacks.

Noise performance

According to datasheet of SR830 LIA, the input referred noise is $6\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 kHz. But the actual observed input noise is much higher than that. The problem does not come from the LIA, but from the long pick-up cable connecting the probe and the input port of LIA. At low frequency, the amplitude of the pick-up signal can be as low as 1μV, and transmitting weak voltage signal via long cables is not preferred from the electromagnetic interference point of view. Both inductive and capacitive coupling introduce excessive noise into the LIA input, degrading the signal to noise ratio significantly. Experiments conducted in weekends in CNDE usually have better quality than that in weekday, due to less power line induced noise in weekends.

Measurement speed

Because of the degraded noise performance, the time constant of LIA must be much higher than necessary to maintain desired data quality, making the entire measurement much slower than expected. A 10 Hz to 10 kHz 31 points scan can take up to 2 hours to complete. If the scan starts from 1 Hz, in some cases it even needs a whole night to complete.

Frequency Range

The SR830 LIA covers frequencies up to 102 kHz, but the Kepco bipolar operational power amplifier works best below 10 kHz. Conducting experiment higher than 10 kHz is difficult with this setup.

Fan Noise

The fan noise from Kepco bipolar operational power amplifier renders the whole lab inhabitable.

Time Domain Capability

This setup has no time domain capability since all signal is modulated into DC signal in digital signal processor (DSP).

The goal of this thesis is to develop a standalone, general purpose ACPD measurement system that provides fast measurement speed, high signal to noise ratio, low cost, low power consumption and capable of performing time domain measurement. The measurement frequency must cover 1 Hz to 100 kHz. The time cost for each frequency scan must not exceed 20 seconds. A typical frequency scan has 41 points from 1 Hz to 100 kHz, with eight frequency distributed logarithmically per decade. For simple conductivity and permeability measurement, the number of points can be reduced for a real world application. But for advanced application such as hardness profile prediction, more points yield a more robust inverse problem solution. To overcome the limitations of commercial ACPD system consisting of a Stanford SR830 and Kepco power amplifier, a custom test system was build . This custom test system integrates all building blocks of commercial ACPD system into one single board.

CHAPTER 2. HARDWARE DESIGN

2.1 Overview of Hardware Design

Since this is the sixth generation of ACPD instrument developed, we name it APS1006 hereafter. The goal is to develop a standalone instrument with ultra-fast scanning capability, covering wider bandwidth and is able to conduct experiment in time domain. The biggest challenge is to increase the measurement speed while maintain or enhance signal to noise ratio of the final result. In table 1.1, we can see that for a 10 Hz to 10 kHz scan, 66 seconds is still too slow for real time applications.

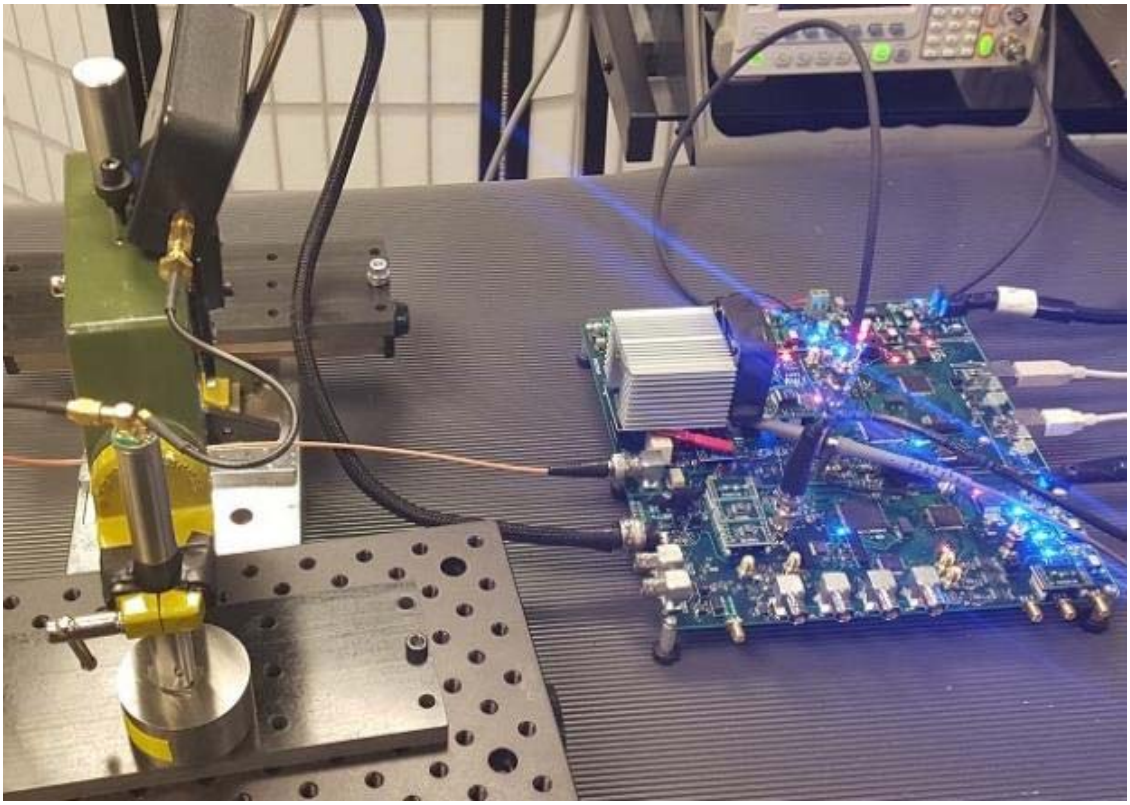


Figure 2.1 ACPD measurement setup using APS1006

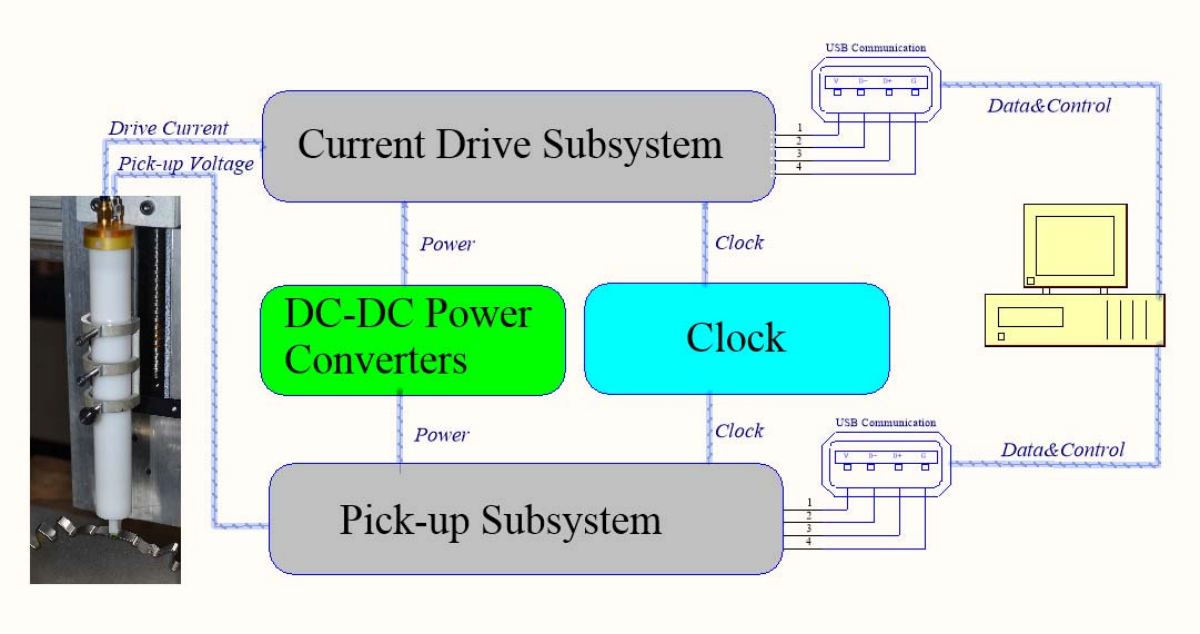


Figure 2.2 Simplified block diagram of APS1006 System

Block diagram shown in Figure 2.2 is analogous to the one in Figure 1.6. But here everything is integrated into a single circuit board rather than using multiple commercially available instruments, and the benefits of doing so are enormous. Please note the diagram in Figure 2.2 is a heavily simplified derivative of the actual diagram.

Two semi-independent partitions

APS1006 diagram can be split into two semi-independent partitions, driver side and pick-up side, which share the same clock source. Section 1.3 mentions that in order to obtain normalized potential drop, it is imperative to make two measurements, one for drive current and the other for pick-up voltage. In this design, these two tasks are handled simultaneously, saving 50% of measurement time instantly. Please also note that these two partitions have their own USB communication channel to the PC.

Driver side

The main task of driver side is to generate voltage signal at required frequency, convert it into current and measure the output current's amplitude and phase. Another feature that is included in the driver side is to generate calibration signal for the pick-up signal chain.

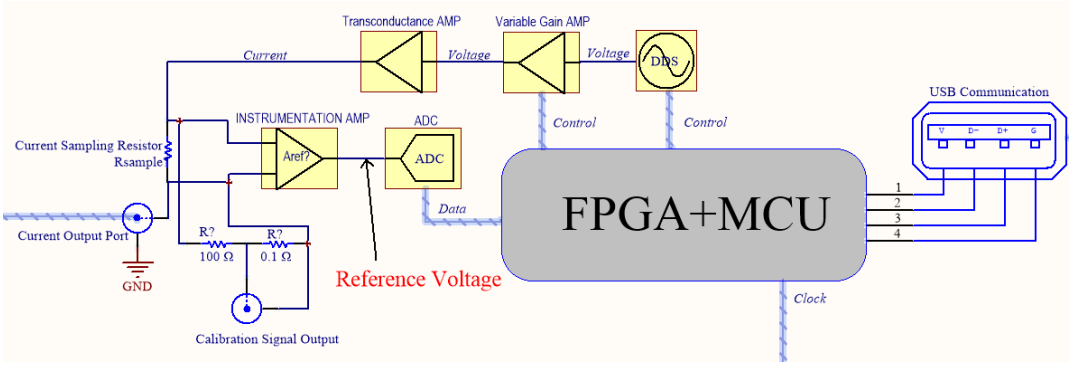


Figure 2.3 Block diagram of driver side

Pick-up side

Pick-up side as suggested by its name amplifies and filters the weak pick-up signal for measurement. Section 1.5 mentions that one of the drawback of the system in Figure 1.6 is that long cable between LIA input and pick-up pins is vulnerable to various kinds of noise. To overcome this shortcoming, a pre-amplifier (not shown in Figure 2.1) is inserted between the four-point probe and the input port of pick-up side, providing polarity toggling (common mode cancellation) and about 67 dB gain.

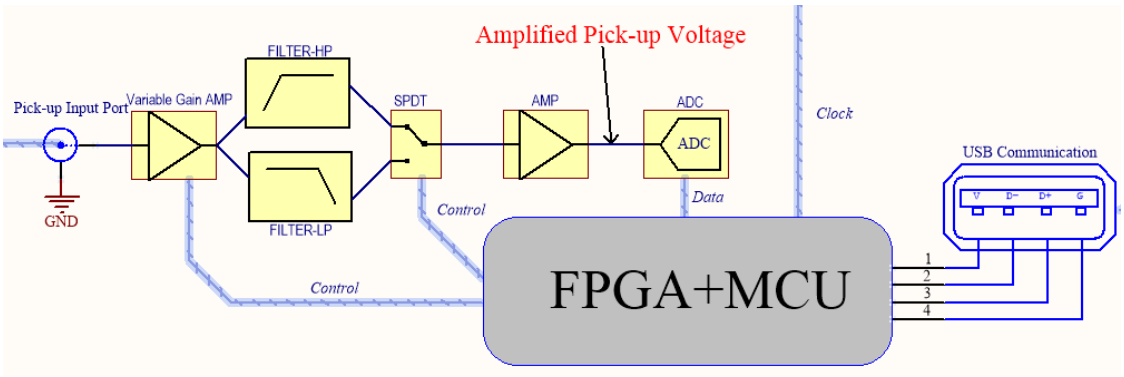


Figure 2.4 Block diagram of pick-up side

Time domain measurement

Since the raw waveform data is available for both drive current and pick-up, APS1006 is also a good platform to perform transient potential drop measurement. Details are covered in chapter four. Table 2.1 lists the detailed function blocks for APS1006, and some of which is discussed in details in later sections.

Table 2.1 APS1006 design details

Item	Content	Notes
1	Direct digital synthesis voltage signal generator and variable gain amplifier	AD9834DDS chip is used for single frequency tone generation. Four LTC2630 DACs are used for multi-tone signal generation.
2	DC-DC power converter for transconductance amplifier	Two stage design. Stage one are switching mode DC-DC regulators for high efficiency buck operation and inverting operation. Stage two are linear regulators for low noise regulation
3	DC-DC power converter for digital circuits	Switching mode regulators only
4	High current transconductance amplifier	Output current amplitude can reach 5 amps at 1 kHz.
5	High speed transconductance amplifier	Output current amplitude can reach 500 mA at 1 MHz
6	Calibration resistor divider	Used to calibrate the pick-up side amplifier chain.
7	Single channel medium speed true bipolar analog to digital converter	For single tone operation data acquisition
8	Low phases noise clock generator	Phase-noise is more important for high frequency measurement.
9	Eight channel switched-capacitor filter bank	Each channel is used to band-pass filter out one frequency in multi-tone operation mode
10	Field-programmable gate array(FPGA)	Part Number: XC6SLX9-2TQG144C

Table 2.1 continued

Item	Content	Notes
11	PIC32 microcontroller	Part Number: PIC32MX795F512L-80I/PT
12	Eight channel low speed ADC	For multi-tone operation data acquisition
13	USB communication for both driver side and pick-up side	Isolated from APS1006
14	High speed analog to digital converter	Not populated for this phase of development.
15	Current output port	BNC port is chosen for backward compatibility.
16	Pick-up input port	Also provides power and control for item 20
17	Digital controlled variable gain amplifier	Extends the dynamic range of the signal conditioning chain
18	Filter banks for pick-up voltage	Different plug-in filters is activated for different frequency band
19	Frequency response test bench	Measure the frequency response of plug-in filter module
20	Pre-amplifier box in figure 2.4	Gain = 67 dB. Differential output for better noise rejection

2.2 APS1006 Design Details

It is not necessary to discuss every bit of detail, but major design decisions that affect the system performance most are covered in this section.

2.2.1 High output current dc-dc regulator

This sub-system is item No.2 in Table 2.1 and its main function is to convert 24V power input to ±7 V and ±5 V for transconductance amplifiers. The maximum dc output current is 6 amps for ±7 V rail, and 1 amp for ±5 V rail. Please note that these two pair of power rails directly power

the transconductance amplifiers, which has a direct connection with pick-up pins, thus it is imperative to make these power supplies as clean as possible. The first step is to convert 24V into ±8 V using adjustable switching mode regulators.

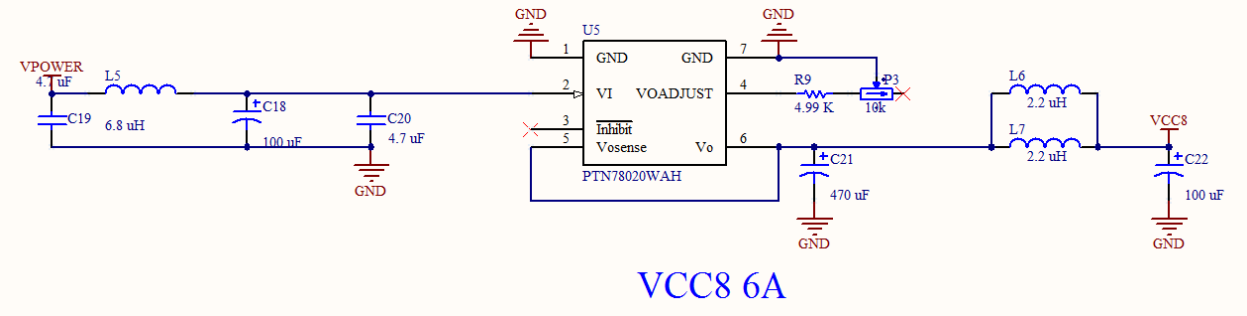


Figure 2.5 Schematic of 24V to 8V 6A regulator

Please note that despite being filtered using inductor L6, L7 and capacitor C22, VCC8 is still quite noisy, which cannot be used to power transconductance amplifiers without further conditioning. This is no surprise because of the switching mode operation of this regulator. Figure 2.6 demonstrates the noise at VCC8 output. Switching noise at this node has an amplitude of 448 mV.

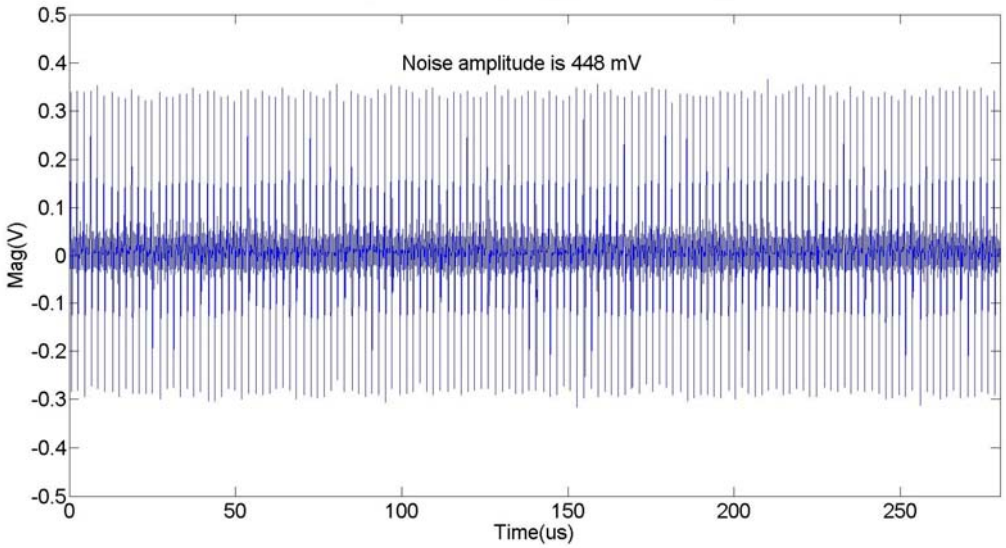


Figure 2.6 Noise at VCC8 output. AC coupled

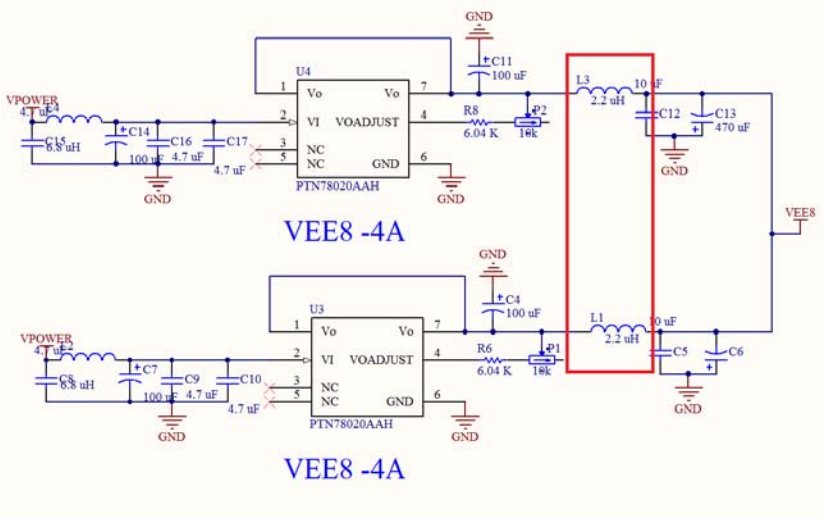


Figure 2.7 Schematic of 24V to -8V 8A regulator

Figure 2.7 is schematic of voltage inverter which generate -8V from +24 V power input. At a first glance, this circuit is wrong due to the fact that the outputs of two independent regulators are tied together. Normally it is not going to work. Inspired by [11], instead of using ballast resistors for load sharing, this design actually takes advantage of DC resistance (DCR) of inductor L3 and L1 for load sharing. Before assembly, make sure that L1 and L3 have the same DCR. If no load sharing is utilized, the invert cannot meet the 6 amp output current requirement since 4 amp is the highest output current for any single inverting regulator in the market at this moment. Similarly, the 424 mV noise amplitude at this node is also not acceptable.

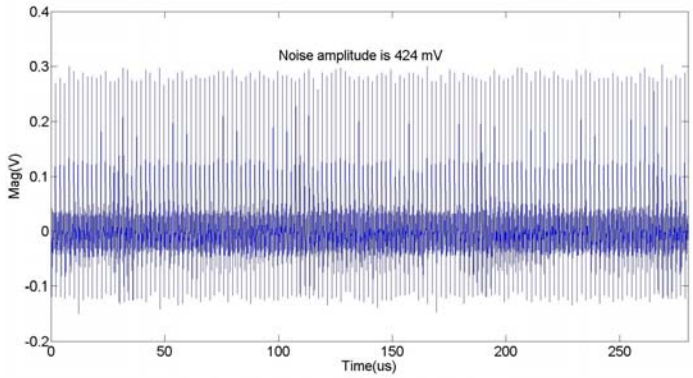
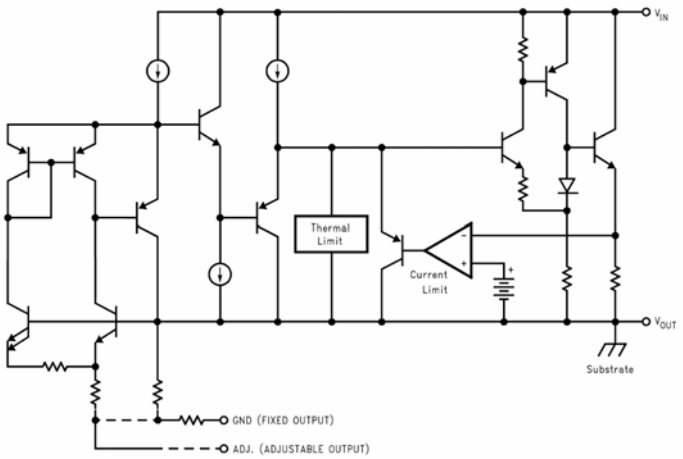
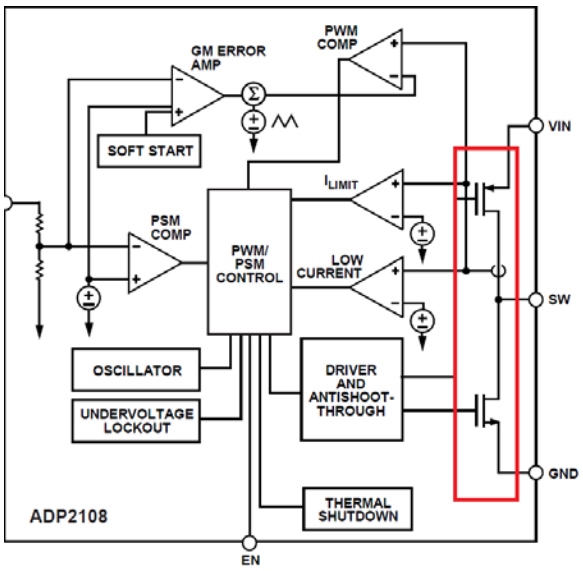


Figure 2.8 Noise at VEE8 output. AC coupled

To clean up the noise at ±8 V power rail. Linear regulators are used. Unlike switching mode regulator, linear regulator generate much less noise and act as a ripple rejecter in this case. Figure 2.9 [12, 13] compares the block diagram of a typical linear regulator and a switching regulator.



(a)



(b)

Figure 2.9 Block diagram of a typical linear regulator (a) and switching regulator (b). In (b), internal switch is emphasized by a red rectangle.

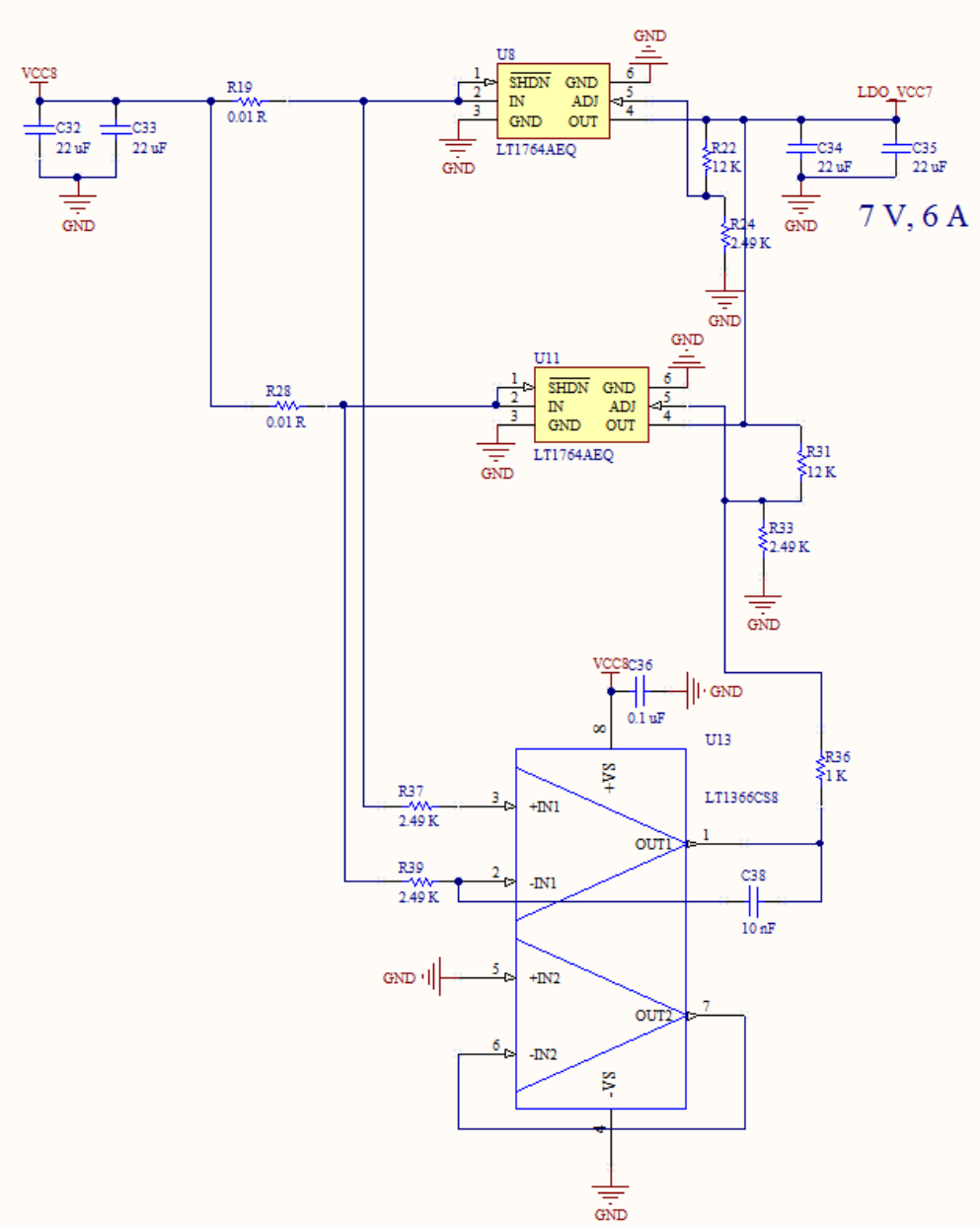


Figure 2.10 Linear regulators for +8 V rail

Two LT1764A linear regulators convert the noisy +8 V to low noises ripple free +7 V. Load sharing is used here again. But the implementation of load sharing is slightly different than before. The goal of load sharing is to make sure for two regulators contribute the same amount of current at fixed output voltage. This must be done by feedback. An accessary operational amplifier U13 is used to this end. Detailed analysis of the circuit is not necessary, but a qualitative analysis is

very helpful. Suppose U8 contribute more current than U11 in Figure 2.10. For U13, pin 3(non-inverting input) will have lower voltage than pin 2(inverting input), generating a negative voltage offset to the pin 5 (feedback input) of U11. Internal feedback loop of U11 makes sure the voltage at pin 5 stay constant by contributing more current to the output. When achieving steady state, the output current from U8 and U11 are equal. Voltage drop due to linear regulator is a trade-off between power supply rejection ratio (PSRR) and power dissipation. One volt (+8 V to +7 V) is selected in this case for good PSRR and reasonably amount of power dissipation.

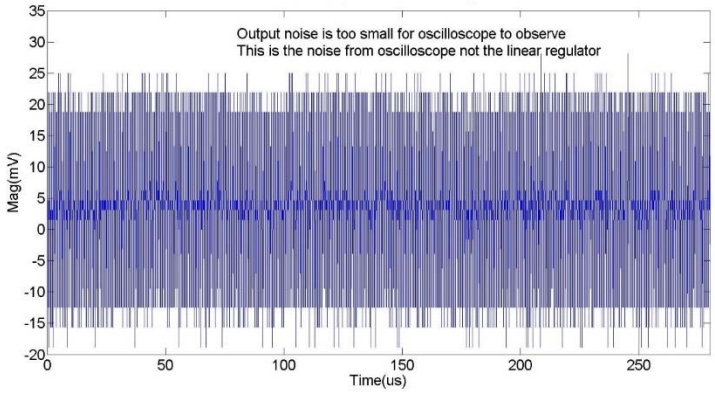


Figure 2.11 Noise at LDO_VCC7 output. AC coupled

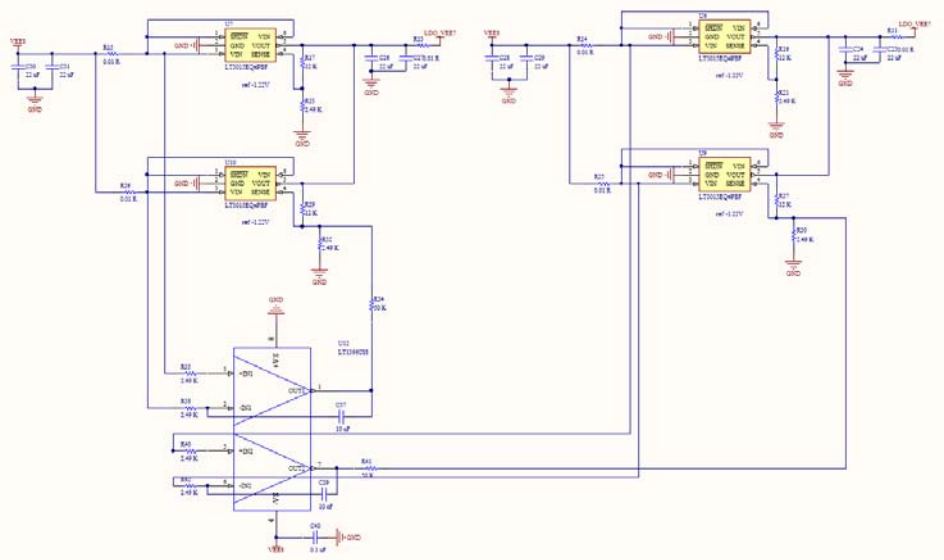


Figure 2.12 Linear regulators for -8 V to -7 V conversion

The maximum current output for a single negative output linear regulator is 1.5 amp. Thus a total of number of four negative linear regulators are used. Load sharing between four independent linear regulators are done by combing two load sharing techniques together. The first tier load sharing adopts the same technique used in Figure 2.10, and the second tier load sharing use conventional ballast resistors method [11]. Noise level at the negative linear regulator output is greatly reduced as well. ±5 V rail can be easily derived from the low noise ±7 V using two linear regulators.

2.2.2 Single tone and multi-tone direct digital synthesis

It is very important to generate a well-controlled waveforms of desired frequency for most electronic test equipment, and APS1006 is no exception. The most flexible method is direct digital synthesis (DDS) [14]. Figure 2.13[15] shows the basic architecture for DDS.

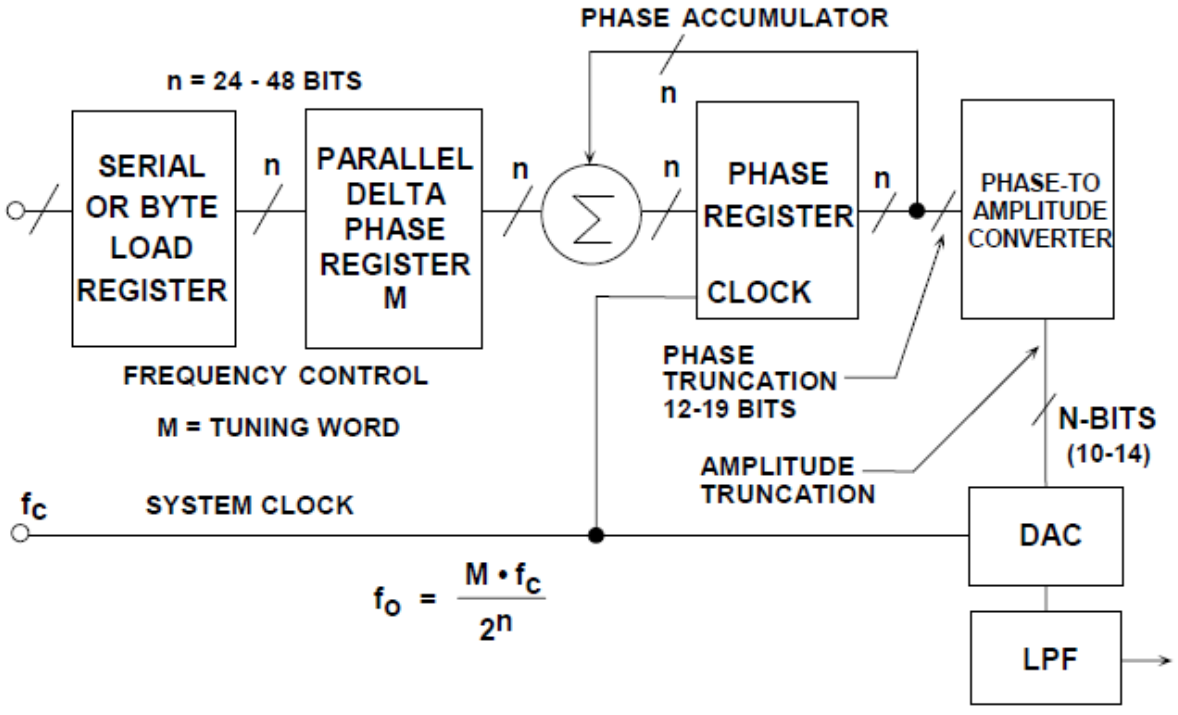


Figure 2.13 DDS architecture

The beauty of this method is that the output frequency is tuning word M times the frequency resolution $\frac{f_c}{2^n}$, where f_c the clock frequency and n is the number of bits of the phase accumulator. In APS1006, AD9834 DDS chip is used which has a clock frequency of 40 MHz and n=28, thus the frequency resolution is $\frac{40\text{MHz}}{2^{28}}$, or 0.149 Hz If 1 MHz output is needed, program tuning word M to 6710886 yields a 0.99999994 MHz actual output frequency. Since DDS system is a sampled data system [15], special attention must be paid to aliasing and filtering. Figure 2.14[15] demonstrates the aliasing in a DDS system.

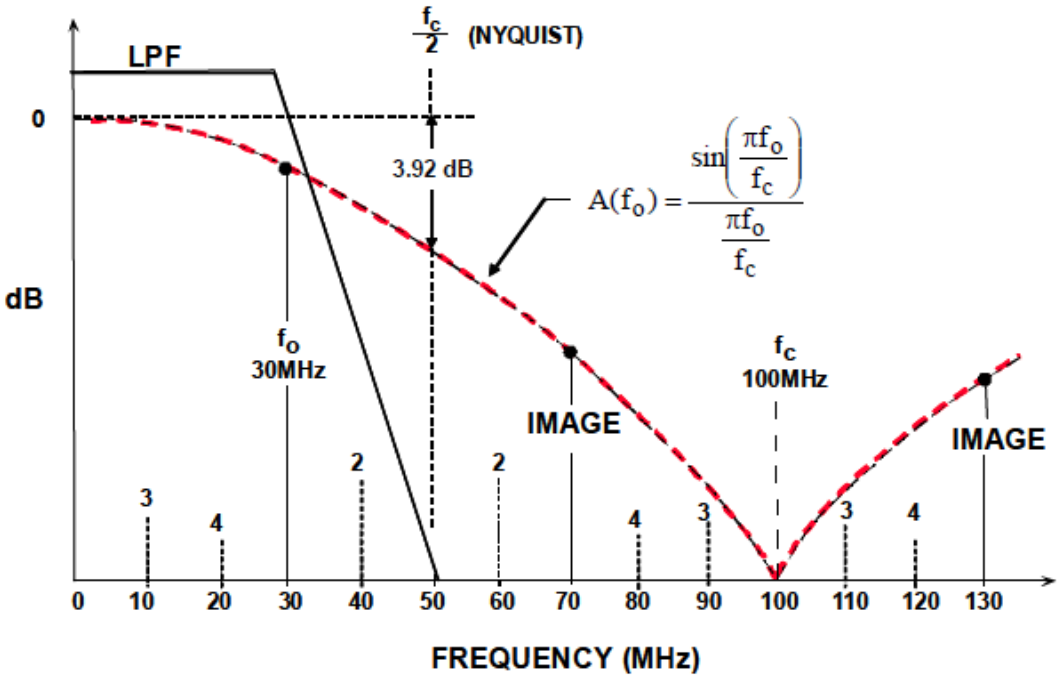
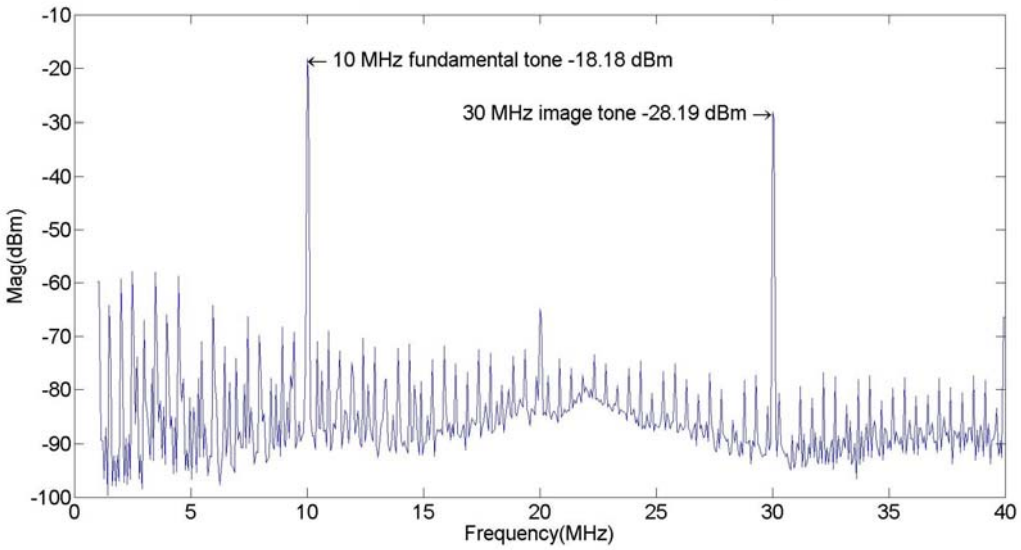
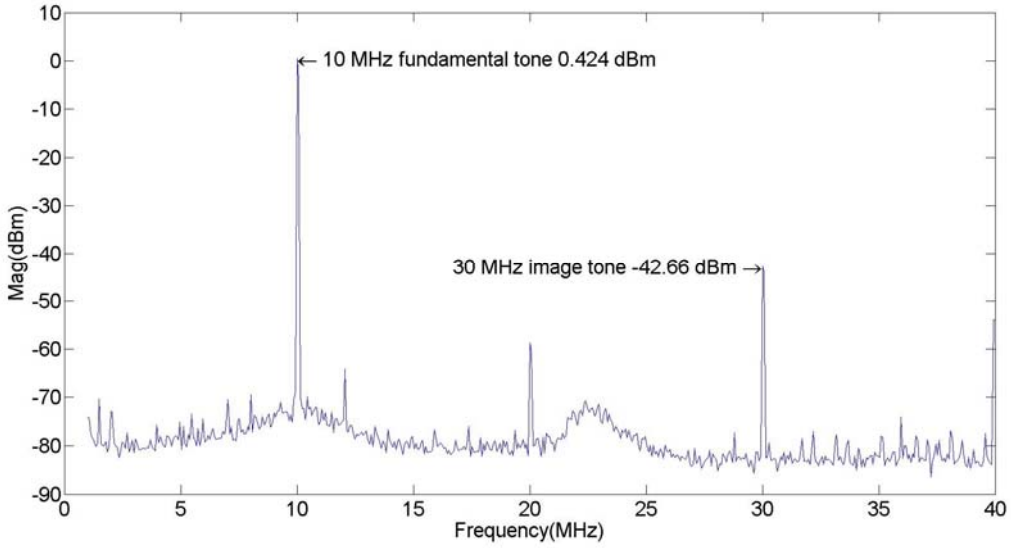


Figure 2.14 DDS aliasing

An antialiasing filter must be used after the reconstruction DAC [15] if the output frequency is close to Nyquist frequency. Figure 2.15 (a) and (b) shows the spectrum of 10 MHz DDS output in APS1006 before and after antialiasing filter.



(a)

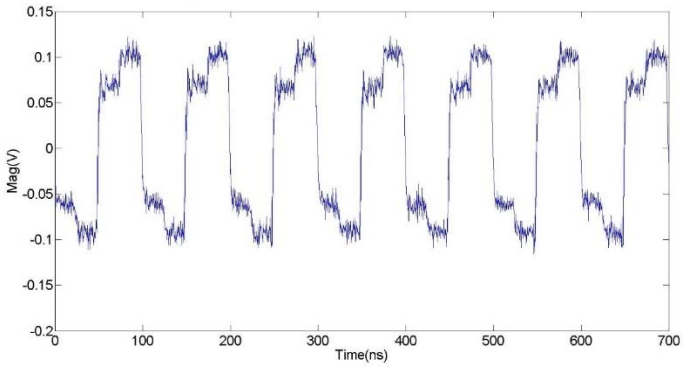


(b)

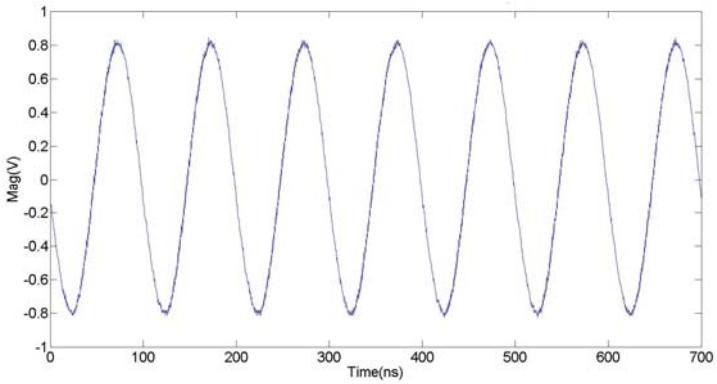
Figure 2.15 Spectrum of 10 MHz DDS output without (a) and with (b) antialiasing filter.

Because 10 MHz is close to 20 MHz Nyquist frequency in this case, SFDR of unfiltered DDS output is very undesirable, indicating a heavily distorted waveform in time domain. Figure 2.16

(a) shows the unfiltered DDS output in time domain, and (b) shows the filtered DDS output in time domain. In APS1006, a fourth order 10 MHz low pass filter approximating a Chebyshev frequency response is used as antialiasing filter.



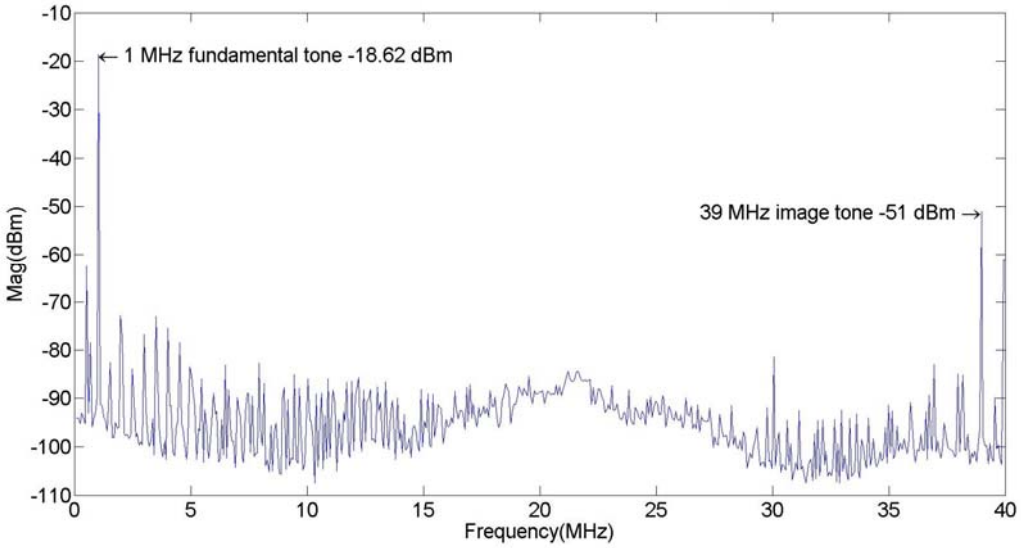
(a)



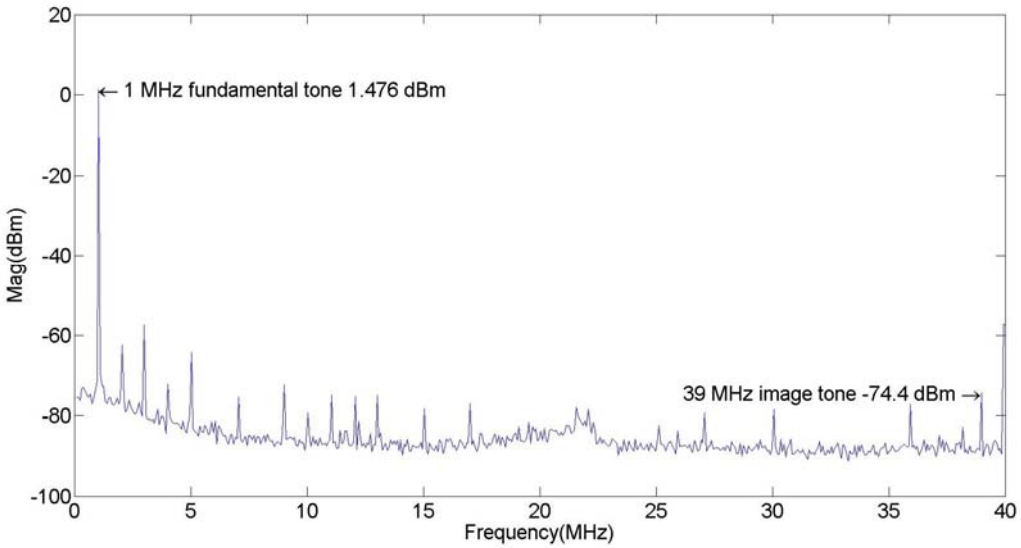
(b)

Figure 2.16 Unfiltered 10 MHz DDS output in time domain (a), and filtered DDS output in time domain (b)

For frequency far away from Nyquist frequency, unfiltered output has much better SFDR due to $\frac{\sin(x)}{x}$ function in Figure 2.14. But antialiasing filter is still necessary.



(a)



(b)

Figure 2.17 Spectrum of 1 MHz DDS output without (a) and with (b) antialiasing filter.

To speed up the measurement of APS1006 at low frequency range, especially from 1 Hz to 100 Hz, it is advantageous to work in multi-tone mode. DDS architecture allows the designer to implement multi-tone voltage signal generation with ease.

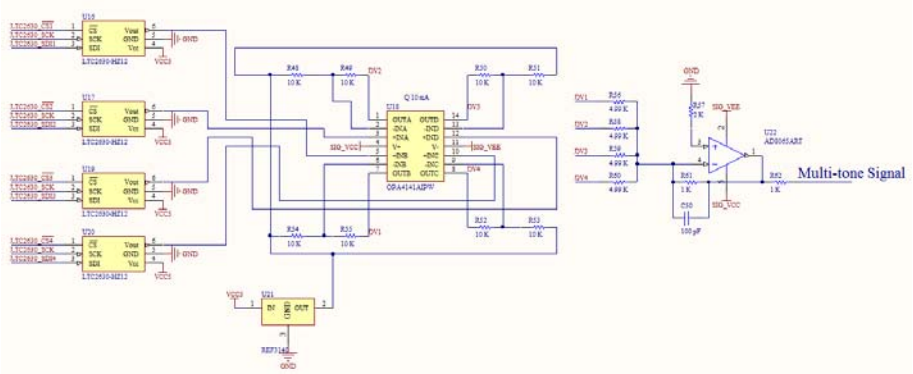
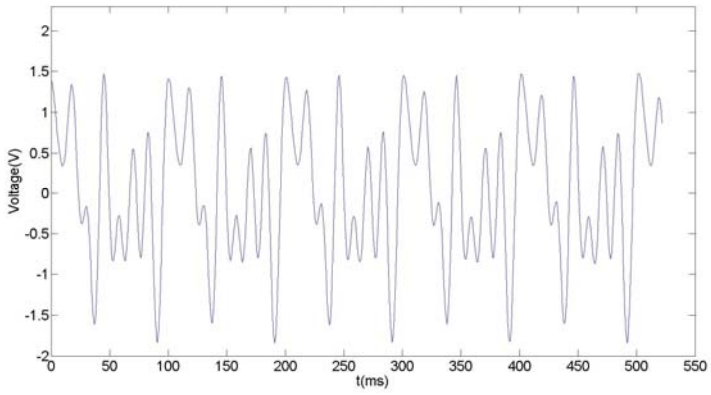


Figure 2.18 Schematic of multi-tone DDS.

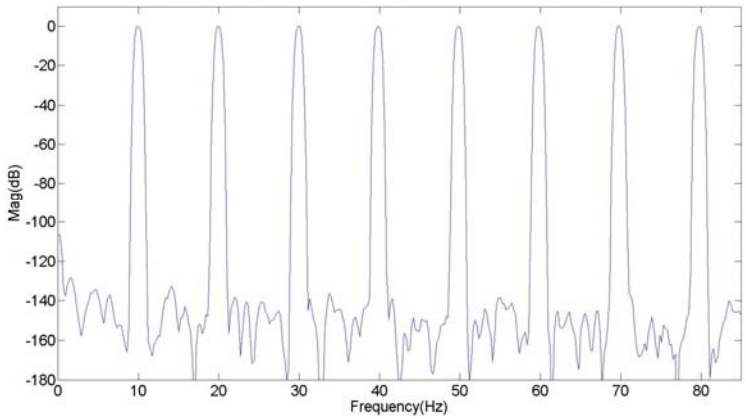
Four independent digital to analog converters (DAC) are used to produce up to eight different frequencies. DAC outputs are centered on 2.048 V, thus an OPA4141 is used to shift the DAC outputs to be centered on 0 V. The following AD8065 acts as inverting adder and antialiasing filter, which outputs multi-tone signal centered on 0 V. All digital operations of DDS are handled by FPGA in item 10 of Table 2.1.

Multi-tone DDS allows APS1006 to measure up to eight frequencies simultaneously, saving tremendous amount of time at low frequency range. Figure 2.19 shows the multi-tone DDS output in time domain and frequency domain.APS1006 contains both AD9834 single tone DDS and custom multi-tone DDS, giving more flexibility to drive voltage generation.



(a)

Figure 2.19 Multi-tone DDS output in time domain (a)



(b)

Figure 2.19 (continued) and frequency domain (b).

Apparently this DDS output contains eight linearly spaced frequencies from 10 Hz to 80 Hz.

2.2.3 Continuously variable linear in volt attenuator

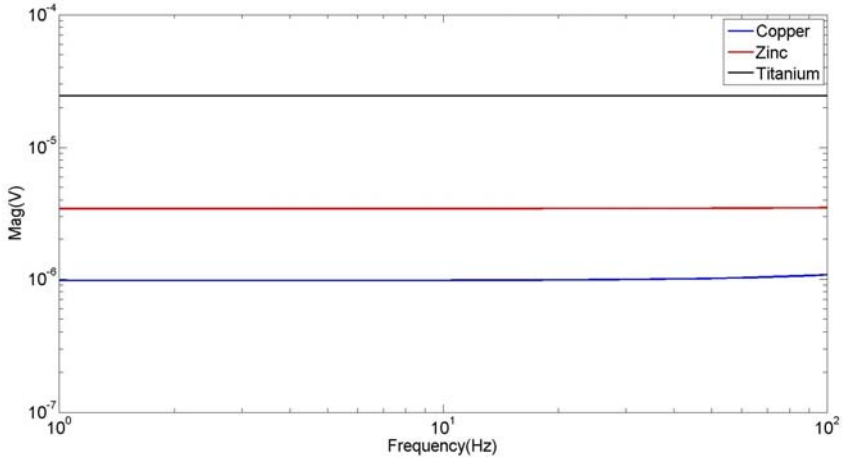


Figure 2.20 Theoretical ACPD calculations for three kinds of metal

Please note that the theoretical ACPD calculation in Figure 2.20 uses the dimension of MK-3 probe. Because of vastly different electrical conductivity, these three materials yield very different potential drop.

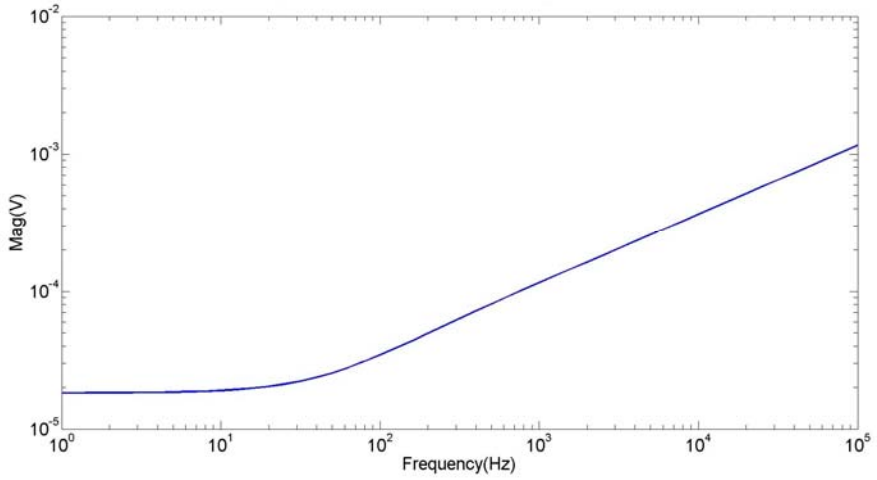


Figure 2.21 Theoretical ACPD calculations for metal from 1 Hz to 10 kHz

Figure 2.21 demonstrates that for a given material, the magnitude of potential drop varies with frequency significantly. Thus the drive current for four-point probe must have enough dynamic range to handle all scenarios. A voltage controlled variable attenuator is desired for this task. Unfortunately, voltage variable attenuator on market are targeted to point-to-point microwave radio, SATCOM, radar, and base station applications [16]. Alternatively, voltage controlled variable gain amplifier may be used. However the gain range of those amplifiers are not desirable, they focus on variable gain, but much needed here is continuously variable loss (attenuation). One of the appropriate solutions is to use a four-quadrant analog multiplier.

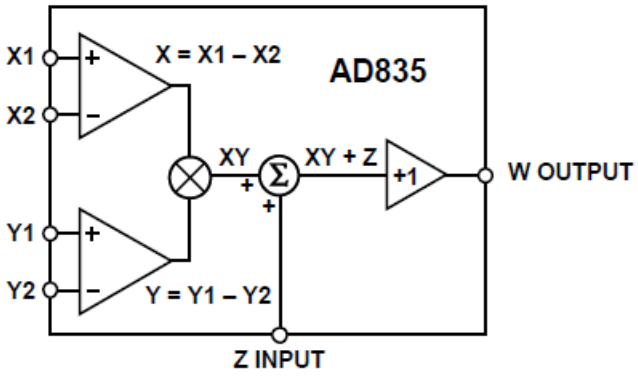


Figure 2.22[17] Block diagram of AD835 multiplier

AD835 is a voltage output four-quadrant multiplier and if one of the input is a DC control signal ranges from 0 V to 1 V, it can be used as a continuously variable linear in volt attenuator. To ensure the linearity of this multiplier, both X and Y inputs are limited to 1 V amplitude.

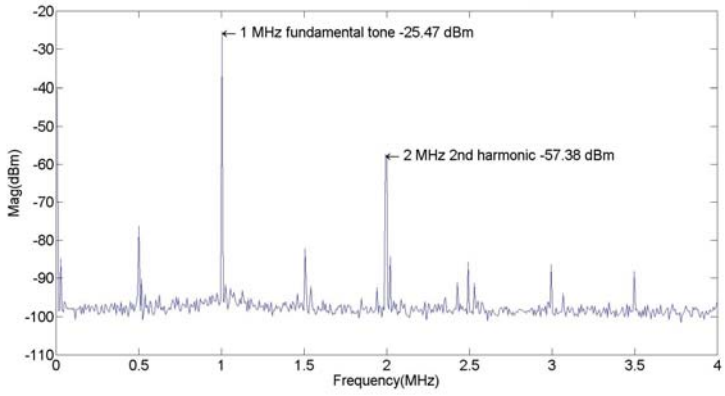
$$X_2 = Y_2 = Z = 0$$

$$X_1 = V_{\text{ctrl}}$$

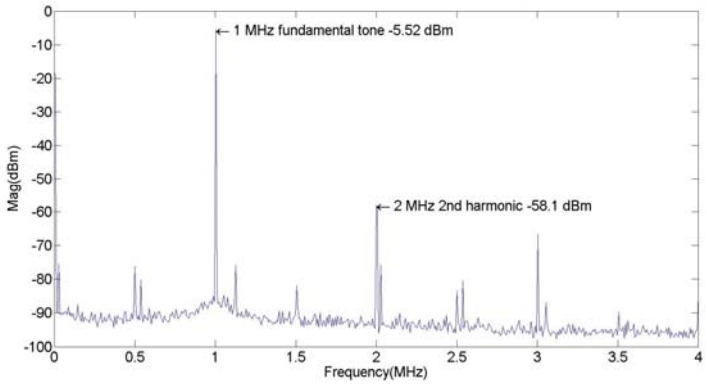
$$Y_1 = V_{\text{DDS}}$$

$$W = (X_1 - X_2)(Y_1 - Y_2) + Z = V_{\text{ctrl}} V_{\text{DDS}} \tag{2.1}$$

Figure 2.23 shows the spectrum of multiplier output W with three different V_{ctrl} settings.

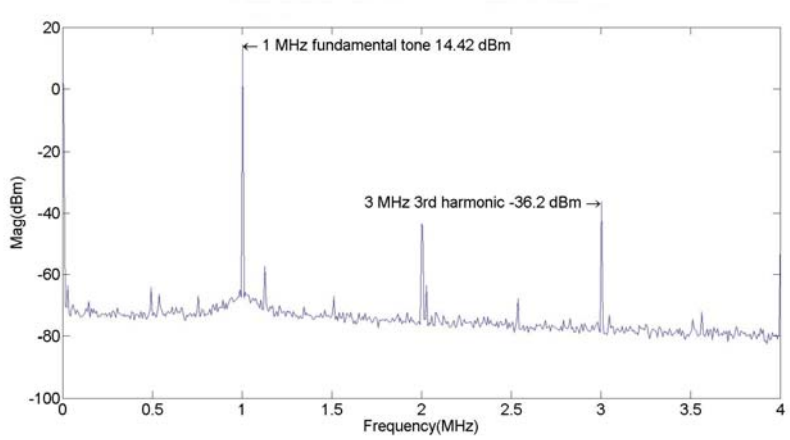


(a)



(b)

Figure 2.23 Spectrum of multiplier output at 1 MHz with 10 mV (a), 100 mV (b)



(c)

Figure 2.23 (continued) and 1000 mV (c) control voltage

The output magnitude is linear with control voltage and has a gain control range of at least 40 dB. Combing this continuously variable linear in volt attenuator with single tone and/or multi-tone DDS signal generator gives APS1006 sufficient flexibility for various kinds of metallic materials at vastly different frequency bands.

2.2.4 Overview of transconductance amplifier

The most important part of driver side of APS1006 is to provide AC driver current for four-point probe. An ideal transconductance amplifier should have high output current (>2 amp in amplitude) and wide bandwidth (up to 1 MHz). But it is very difficult if not impossible to design and implement a transconductance amplifier like that. Referring to Figure 2.21, it is easy to see that high current is more necessary for frequency lower than 1 kHz. Thus we can implement two types of transconductance amplifiers, one has high output current but narrower bandwidth, and the other has less output current but wider bandwidth. A mechanical relay determines which of the two transconductance amplifiers are activated as shown in Figure 2.24.

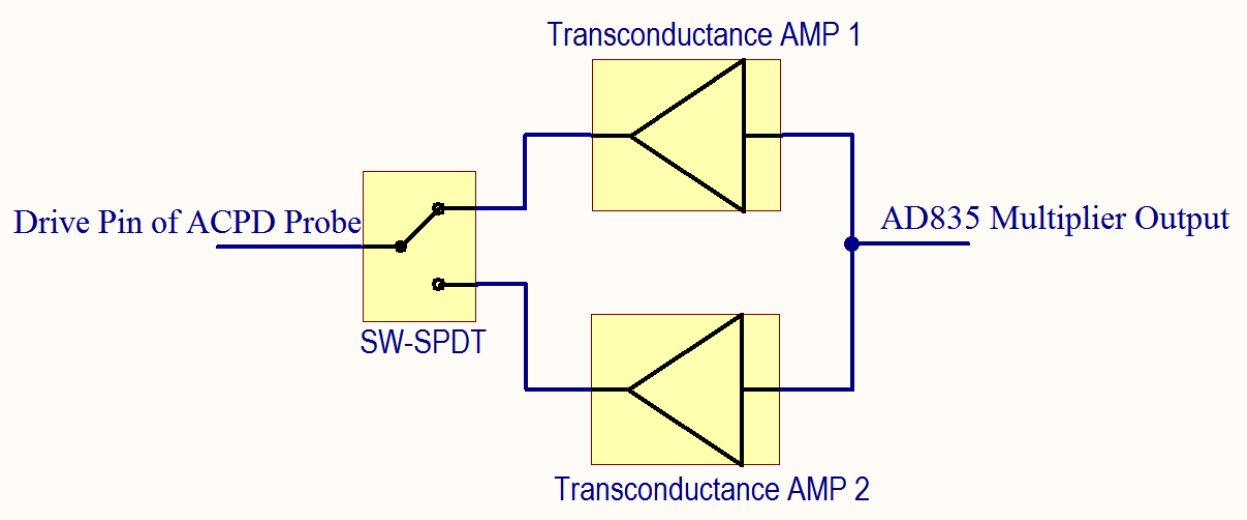


Figure 2.24 Block diagram of transconductance amplifiers pair

There are three configurations worth considering for the transconductance amplifiers. During the development of legacy versions, extensive research has been done to investigate the pros and cons of each type of configuration, which are summarized here.

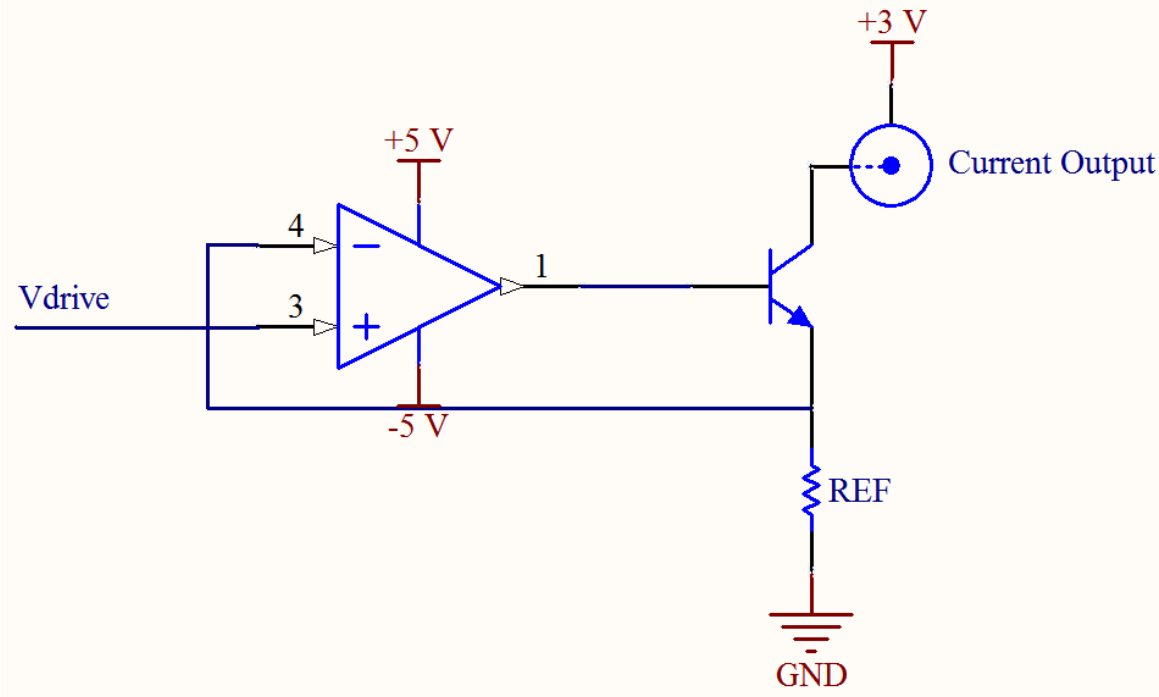


Figure 2.25 Schematic of configuration one for transconductance amplifiers

Assuming it is stable, the output current is $\frac{V_{\text{drive}}}{\text{REF}}$. This configuration is used in the first generation to the third generation systems in table 1.1. The operational amplifier (ADA4851-1) is a high speed, rail-to-rail output operational amplifier [18], while the power transistor (ZXTN25012EZ) is a 12V NPN high gain transistor that can withstand 6.5 amp continuous current [19]. Actual output current of the transistor (500 mA maximum) is limited by the thermal resistance of its SOT89 package.

Three drawbacks rule this configuration out for APS1006:

1. Power efficiency is low due to its Class A operation. Maximum output current is limited.
2. Stability is hard to maintain because of the additional pole associate with the power transistor.
3. At quiescent point the probe voltage is 3 V, which compresses the input linear swing range of low noise amplifier on the pick-up side.

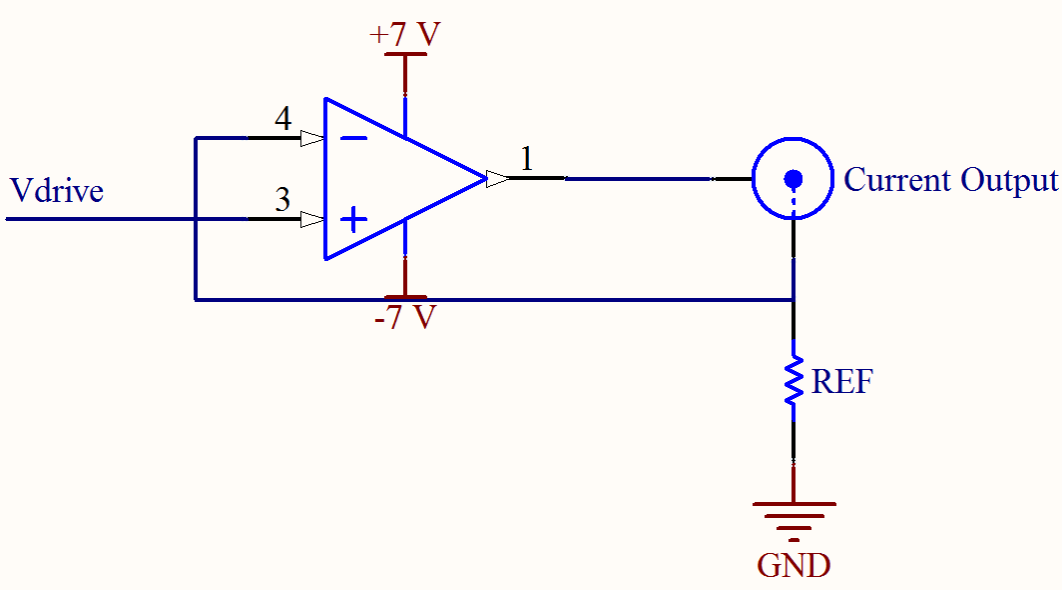


Figure 2.26 Schematic of configuration two for transconductance amplifiers

Similar to configuration one, the output current is still $\frac{V_{\text{drive}}}{\text{REF}}$. The operational amplifier is no longer a general purpose one because in this configuration it is the operational amplifier itself supply output current to the probe. High-current operational amplifier OPA548 is a good candidate for this schematic. This configuration is more desirable than configuration one because of its Class AB operation mode, which has better power efficiency intrinsically, allowing higher maximum output current. And the pole associate with power transistor is gone, making the configuration less prone to potential stability problem. Despite significant improvements, this configuration is still not the best choice. One inconspicuous drawback is that the common mode voltage seen by the pre-amplifier on pick-up side equals V_{drive}, which increases overall common mode error. Another minor shortcoming is that the load is not grounded, causing inconvenience when implementing block diagram in Figure 2.24.

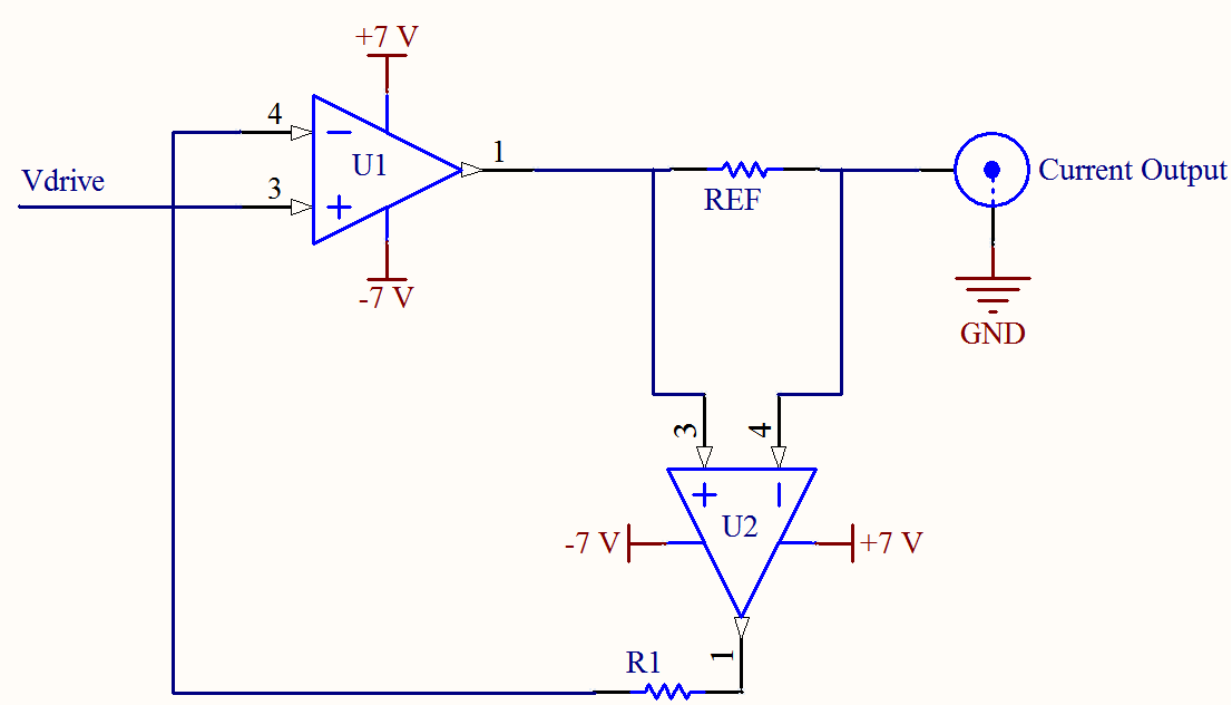


Figure 2.27 Schematic of configuration three for transconductance amplifiers

Configuration three is similar to configuration two but a secondary high speed instrumentation amplifier U2 is inserted into the feedback loop. U2 senses the voltage across REF resistor and feedback this signal to the inverting input of high current output power amplifier U1. When stable, the current output is $\frac{V_{\text{drive}}}{\text{A REF}}$, where A is the gain of U2.

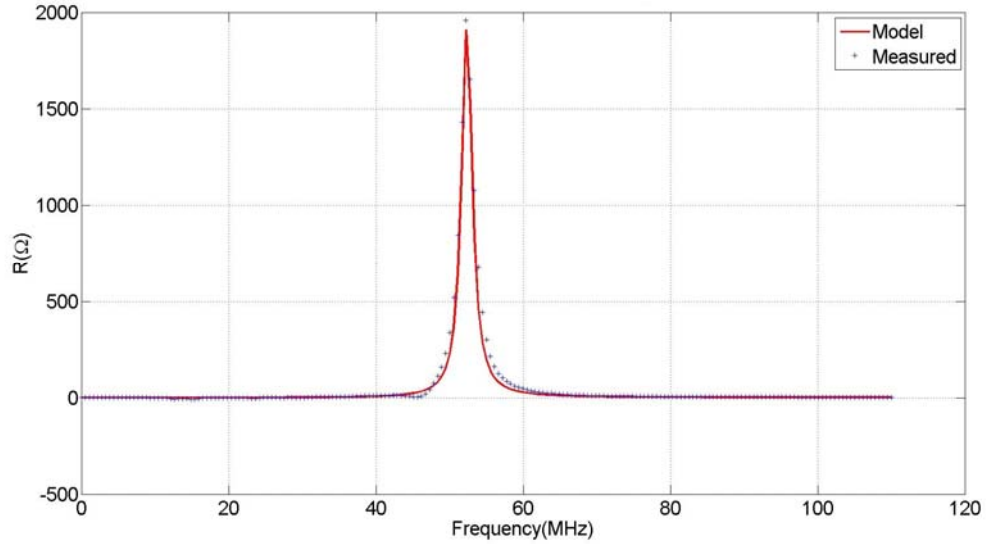
This configuration is selected for APS1006 because of its main advantages:

1. Class AB operation gives rise to higher power efficiency, compared with configuration one.
2. Common mode error is reduced to minimum compared with configuration two. The source of common voltage of this configuration comes from the finite resistance of cables only. Common mode voltage seen by pre-amplifier on pick-up side is minimized.
3. Load is grounded for easier integration of multiple transconductance amplifiers.

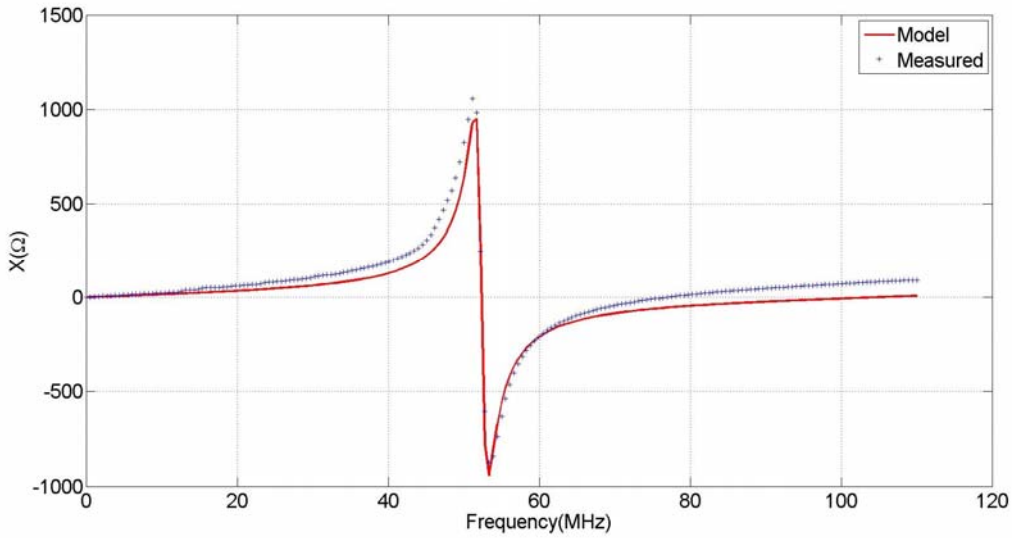
The added instrumentation does introduce another pole in the feedback loop, thus care must be taken to ensure the stability of this configuration. The impedance looking into the drive pins plays an important role in terms of transconductance amplifier stability. As seen in Figure 2.4, a coaxial cable connects current output port in APS1006 board to drive pins of the probe, thus the input impedance can be modeled as lossy transmission line [20]

$$Z_{\text{in}} = Z_0 \frac{\alpha l \cos(\beta l) + j \sin(\beta l)}{\cos(\beta l) + j \alpha l \sin(\beta l)} \tag{2.2}$$

Agilent impedance analyzer 4294A is used to measure this impedance from 40 Hz to 110 MHz and Figure 2.28 compares the measured result and model.



(a)



(b)

Figure 2.28 Real part (a) and imaginary part (b) of ACPD probe drive pin input impedance

This lossy transmission line model will be helpful when analyzing transconductance amplifier stability. In the frequency of interest (DC to 100 kHz), the input impedance is inductive, which adversely affects the stability of transconductance amplifier.

2.2.5 High current transconductance amplifier

The high current transconductance amplifier mainly focus on frequencies from DC to 1 kHz.

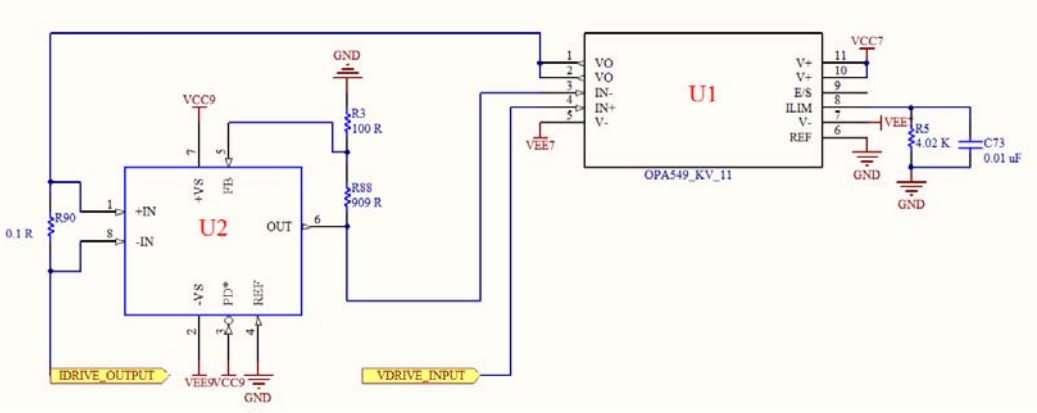


Figure 2.29 Schematic of high current transconductance amplifier

This schematic is based on configuration 3 of Figure 2.27. U1 is OPA549, a high-current operational amplifier with gain bandwidth product of 900 kHz, supporting 8A continuous current output. U2 is AD8130, a 270 MHz differential amplifier. Drive voltage input connects to the non-inverting pin of U1. Reference resistor R90 is in series with current output, converting output current into a differential voltage. U2 converts the differential voltage into a single-ended voltage and feedback the single-ended voltage to the inverting input of U1, completing the feedback loop. Assuming stable, the single-ended voltage on inverting input pin must equal to the drive voltage on non-inverting input pin. The amplifier then acts as a transconductance amplifier. Please note that the differential amplifier U2 has a gain of 10, thus the transconductance of this amplifier is $\frac{1}{10*R90} = \frac{1}{10*0.1} = 1\ Siemens$. The gain of U2 effectively amplifies the reference resistor R90's value by 10. For a given transconductance, doing this yields a more thermal stable circuit. If the gain of U2 is one, to achieve the same transconductance, R90 must be 1 Ω instead of 0.1 Ω. When the amplifier outputs high current, the heat dissipated on R90 decreases the transconductance of

the amplifier due to its positive temperature coefficient (TCR). However, without compensation, this configuration is inherently unstable due to the inductive input impedance of ACPD drive pins stated in section 2.2.4.

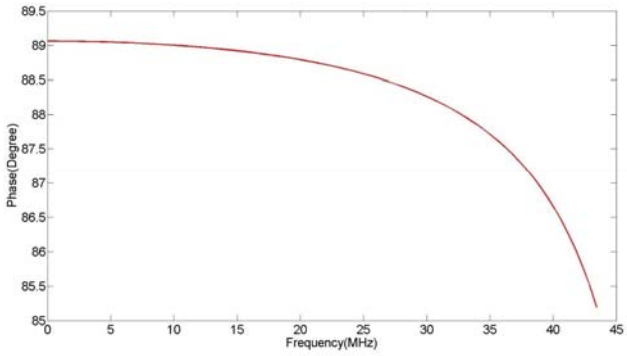


Figure 2.29 Phase of ACPD drive pin input impedance

Because of the nearly pure inductive input impedance (load impedance for this amplifier), the associated phase shift approaches 90°. The phase margin of a typical operational amplifier is always less than 90°, thus without proper compensation, this configuration has insufficient phase margin, as shown in the waveform captured by oscilloscope below.

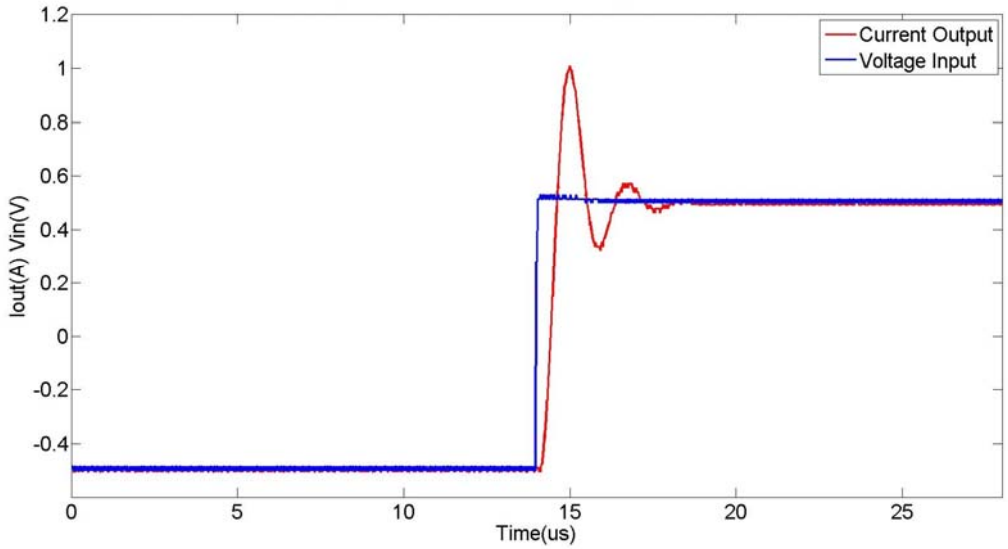


Figure 2.30 Uncompensated transconductance amplifier step response

Figure 2.31 shows the schematic of transconductance amplifier with compensation network.

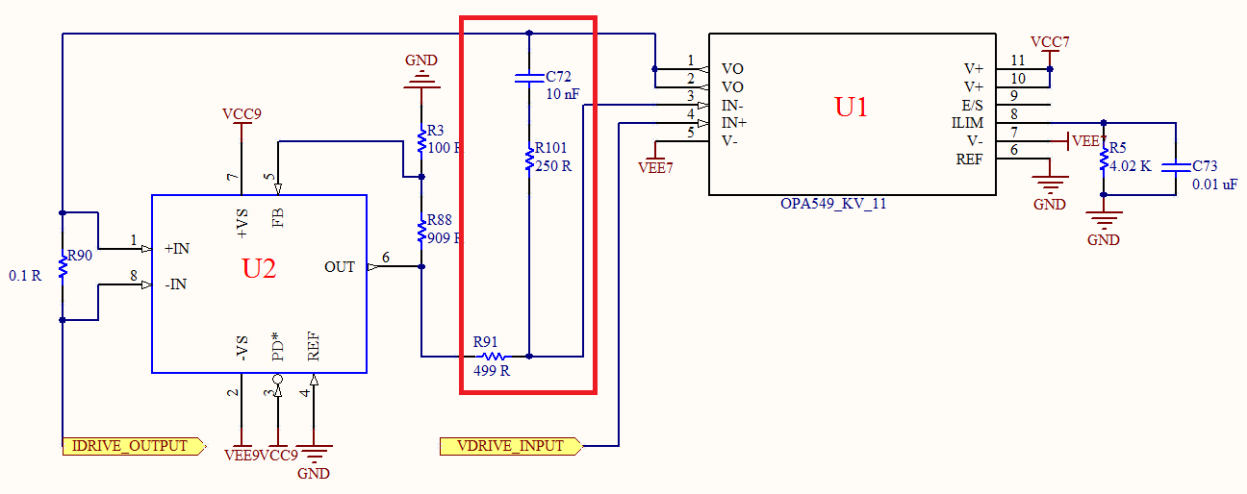


Figure 2.31 Compensation network in transconductance amplifier

The compensation network is inspired by feed-back-lead compensation [21]. At low frequency, C72 is open so the normal operation of transconductance amplifier is not affected. At high frequency, compensation network alters the feedback scheme from current feedback to direct voltage feedback. Direct voltage feedback has no 90° phase lag, thus the phase margin can be significantly improved. Captured oscilloscope waveforms are in Figure 2.32.

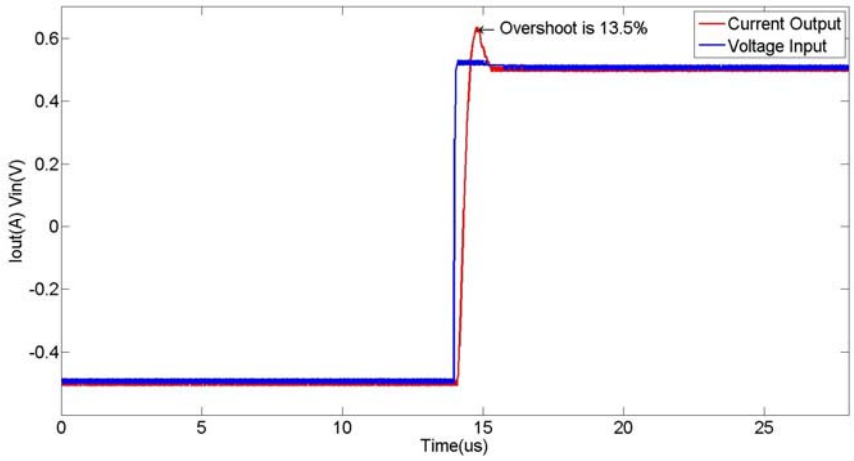


Figure 2.32 Compensated transconductance amplifier step response

The overshoot is 13.5% and according to [22], the phase margin is approximately 55°

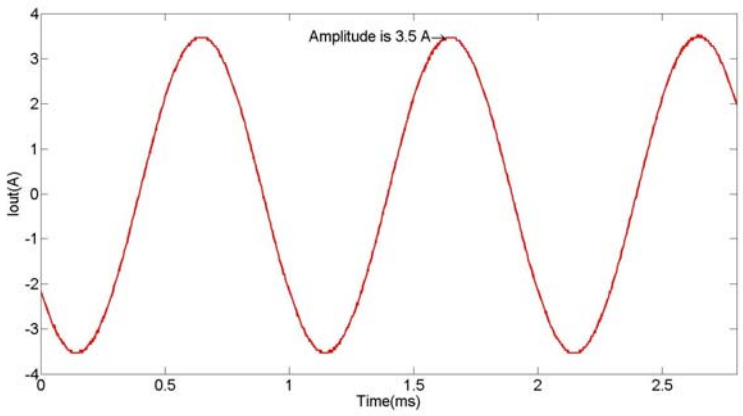


Figure 2.33 High current transconductance delivering 3.5 A current at 1kHz

The maximum current output limit of 3.5A is due to relatively low dc supply voltage ($\pm 7V$). If higher voltage were allowed, larger current output could be achieved. Lower supply voltage is preferred in this case because of thermal stability concern.

2.2.6 Wide bandwidth transconductance amplifier

The wide bandwidth transconductance amplifier mainly focus on frequencies from 1 kHz to 1 MHz

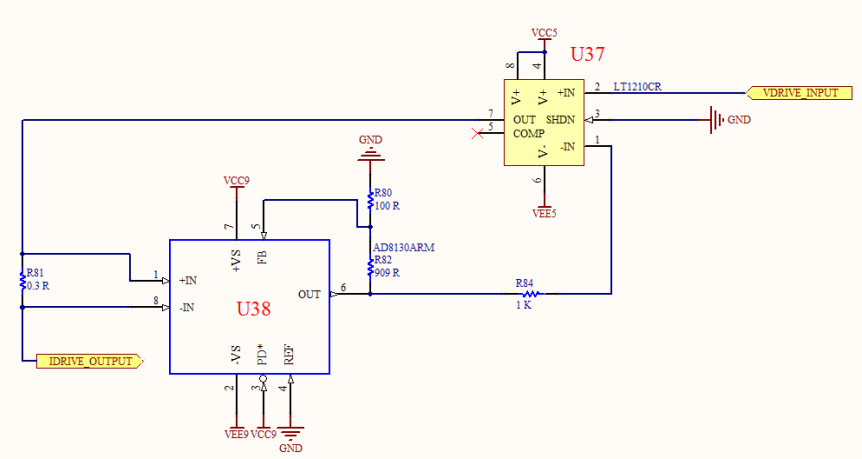
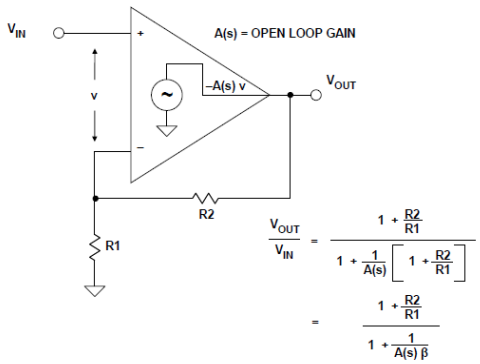
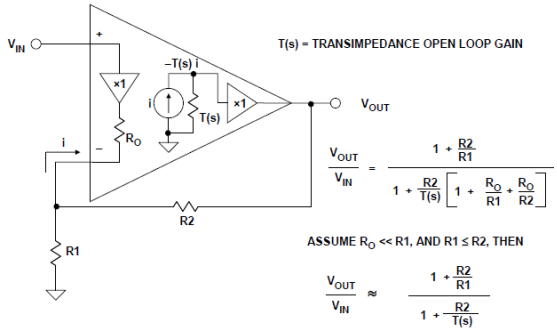


Figure 2.34 Schematic of wide bandwidth transconductance amplifier

Similar to Figure 2.29, this schematic is also based on configuration 3 of Figure 2.27. The biggest difference is that U37 is no longer a high current output voltage feedback operational amplifier OPA549, it is a high speed current feedback operational amplifier LT1210. U38 is AD8130, a 270 MHz differential amplifier, the same amplifier used in Figure 2.29 for the same task. The transconductance of this setup is $\frac{1}{10*\mathrm{R81}} = \frac{1}{10*0.3} = 0.333\ Siemens$. LT1210 Current feedback operational amplifier is preferred for wide bandwidth application because it has high output current, high slew rate and is able to deliver power at frequencies up to 2 MHz [23]. Figure 2.35 [24] compares the basic topologies of conventional voltage feedback (VFB) and current feedback (CFB) operational amplifier.



(a)



(b)

Figure 2.35 VFB (a) and CFB (b) topology comparison in noninverting configuration

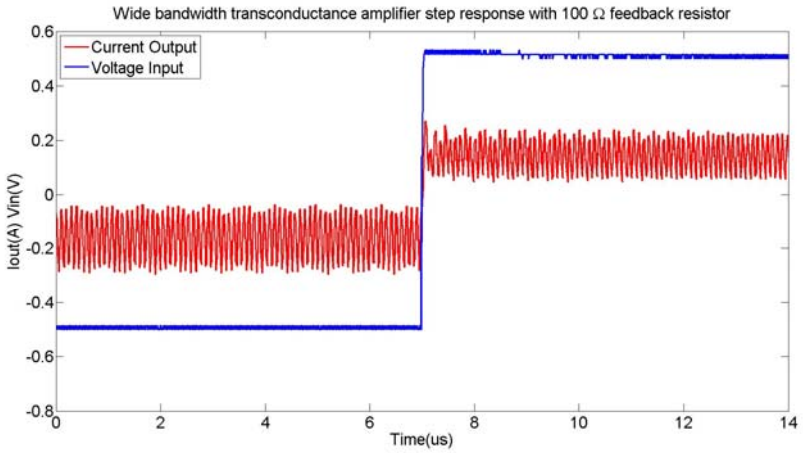
The structure of a VFB amplifier is straight forward. For an ideal VFB amplifier, the input impedance and open loop gain $A(s)$ are infinite high and the output impedance is zero. Please note that for VFB amplifier, the inverting input (one with minus sign) and non-inverting input (one with plus sign) are symmetrical. In Figure 2.35 (b), CFB amplifier's noninverting input is followed by a unity gain buffer, thus noninverting input has high input impedance similar to VFB amplifier's input. The inverting input connects to the output of noninverting input buffer, thus the inverting input has a very low input impedance R_0. The error current i into inverting input controls a transimpedance $T(s)$, whose output is buffered and connected to the output of the CFB amplifier. An ideal CFB amplifier has infinite large transimpedance $T(s)$. Please note that CFB amplifier has asymmetrical inputs, the input impedance of non-inverting and inverting inputs are different. As shown in Figure 2.35, even though the structure of those two types of amplifier are different, the close loop gain is identical if certain assumptions are met.

Table 2.2 Comparison of non-inverting VFB and CFB amplifier equations

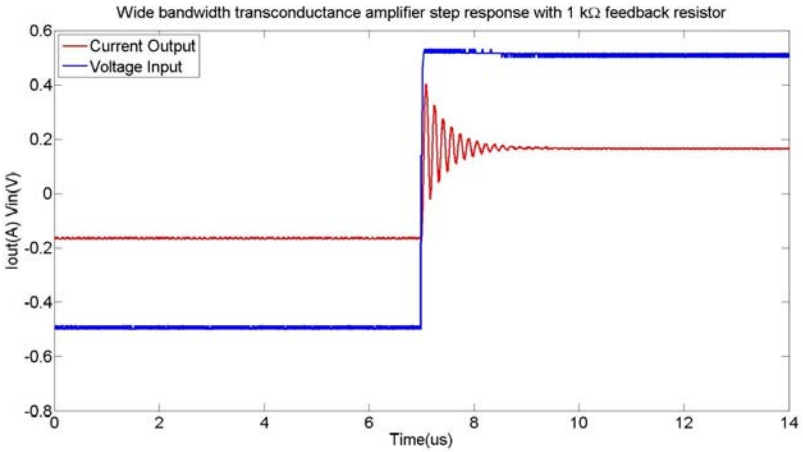
	VFB	**CFB**
Open loop gain	$A(s)$	$T(s)$
Loop gain	$A(s)\frac{R_1}{R_1+R_2}$	$\frac{T(s)}{R_2(1+\frac{R_0}{R_1R_2}(R_1+R_2))}$ [25]
Ideal close loop gain	$1+\frac{R_2}{R_1}$	$1+\frac{R_2}{R_1}$

For a fixed close loop gain, or fixed $\frac{R_2}{R_1}$ ratio, the VFB amplifier's loop gain is always fixed, while the CFB's loop gain is a function of R_2 or R_1 value. Loop gain determines the feedback stability,

thus for CFB amplifier, stable circuit can always be achieved by selecting appropriate feedback resistor value without using external compensation network. Larger resistor value leads to lower loop gain, and therefore it is more likely to be stable. In Figure 2.34, R84's value determines the stability of this circuit. Increasing the value of feedback resistor R84 improves phase margin, at the cost of smaller bandwidth. Figure 2.35 compares the step response of wide bandwidth transconductance amplifier with four different feedback resistor values.

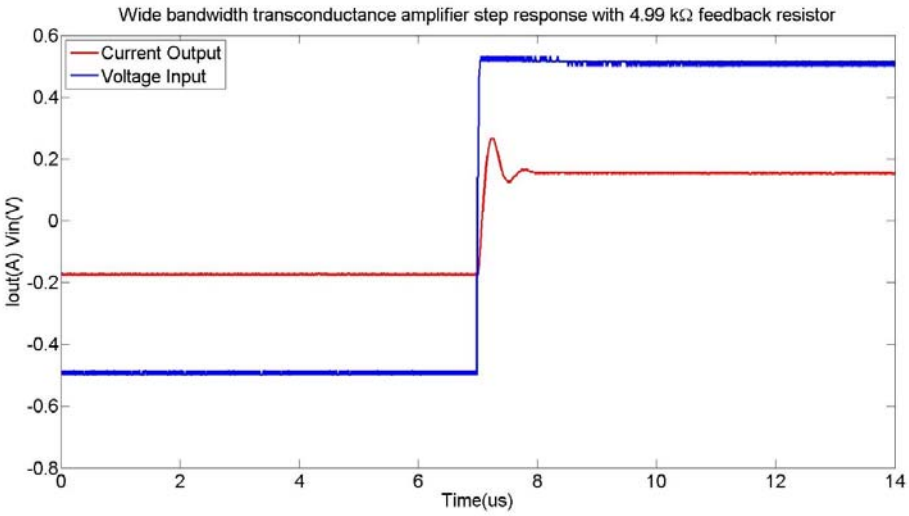


(a)

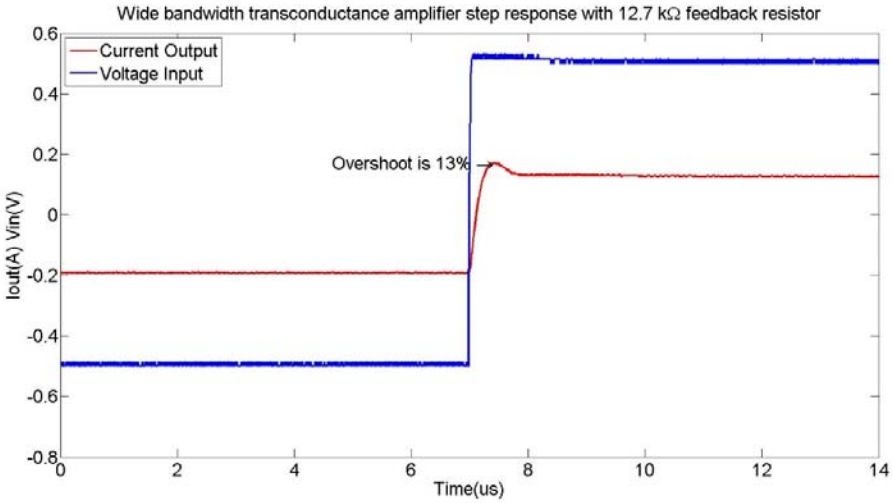


(b)

Figure 2.35 Wide bandwidth transconductance amplifier step response with (a) 100 Ω, (b) 1 kΩ



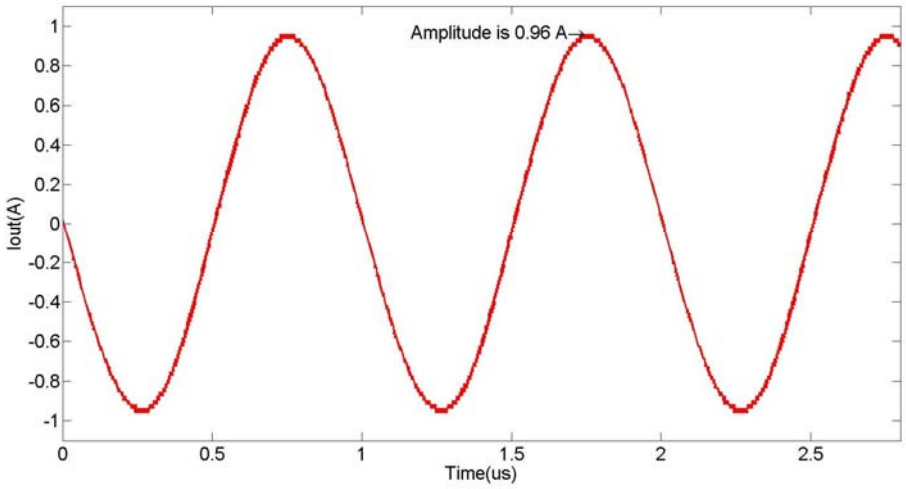
(c)



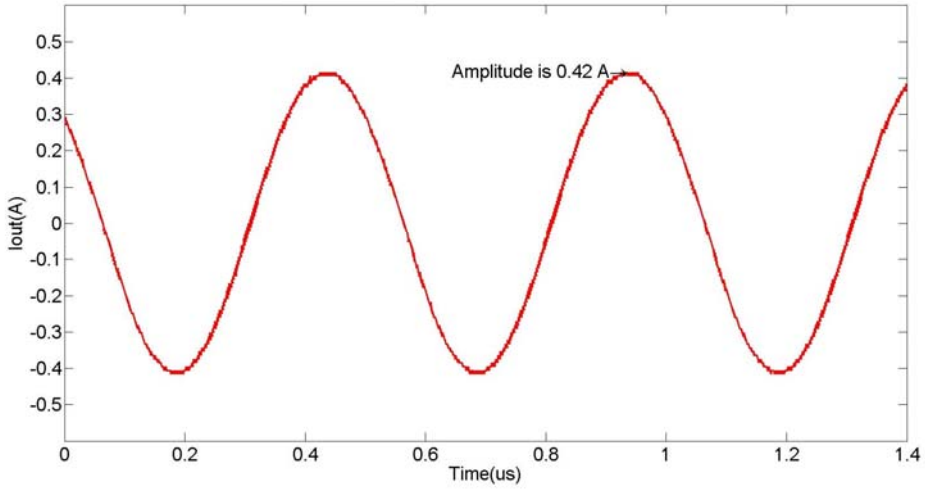
(d)

Figure 2.35(continued) (c) 4.99 kΩ and (d) 12.7 kΩ feedback resistor

In Figure 2.35 (a), 100 Ω feedback resistance is too small to make the circuit stable, resulting self-oscillation. Figure 2.35 (b) (c) (d) demonstrate that larger feedback resistor yields more stable circuit. It turns out that with 12.7 $k\Omega$ feedback resistor, the circuit has 13% step response overshoot or 56° phase margin.



(a)



(b)

Figure 2.36 Wide bandwidth transconductance amplifier maximum current at 1 MHz (a) and 2 MHz (b)

As seen in Figure 2.36, this current feedback wide bandwidth transconductance amplifier is able to deliver 0.96 A at 1 MHz and 0.42 A at 2 MHz, which is sufficient for a broad range of ACPD material characterization applications.

In summary, section 2.2.5 and 2.2.6 discuss the design and test of high current and wide bandwidth transconductance amplifier based on VFB amplifier OPA549 and CFB amplifier LT1210 respectively. Two different techniques for stabilization are used, both achieve good result. The phase margin of those two types of transconductance amplifiers are at least 55°. Table 2.3 lists recommended operational amplifiers for voltage to current conversion. Designer can select appropriate ones according to current output capability and bandwidth requirements.

Table 2.3 Recommended operational amplifiers for voltage to current conversion

Part Number	Topology	Max. Current	Bandwidth
OPA549	VFB	6 A	1 kHz
OPA548	VFB	3 A	1 kHz
OPA564	VFB	1.2 A	500 kHz
LT1210	CFB	1 A	1 MHz
LT1206	CFB	0.2 A	5 MHz
OPA2670	CFB	0.3 A	10 MHz

For very high frequency transconductance amplifier (BW$\geq 5\ MHz$), it is recommended to place the transconductance amplifier in active probe analog front end sub-assembly (item No.20 in Table 2.1) rather than in the main circuit board because of stability concern. Detailed discussion on this topic is not in the scope of this dissertation.

2.2.7 Continuous time low-pass filter

The most important task for the pick-up side is to amplify and filter the weak pick-up signal so that it is suitable for analog to digital converter's input. The low noise amplifiers (item No.20 in Table 2.1) has a gain of 66.5 dB and 3 dB bandwidth of 195 kHz, as shown below

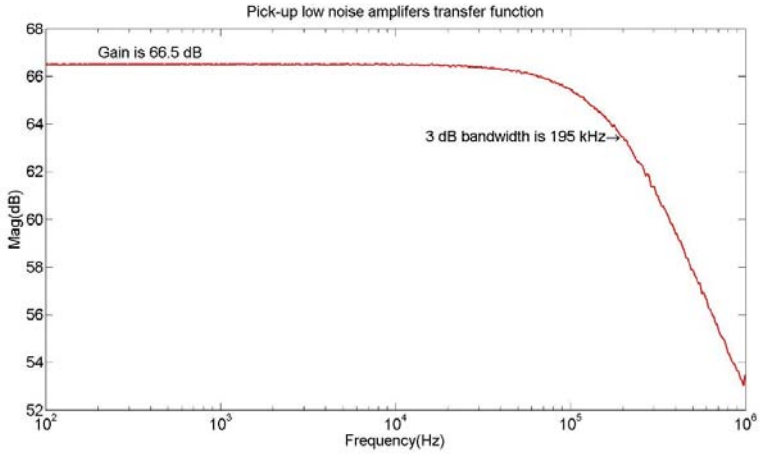
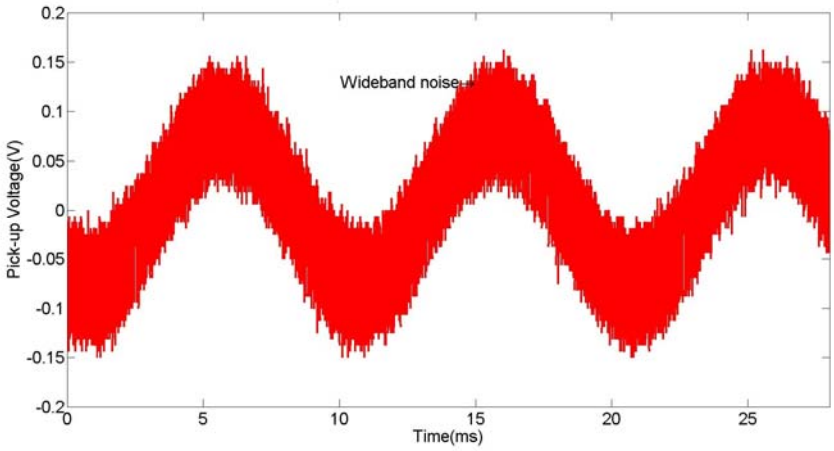


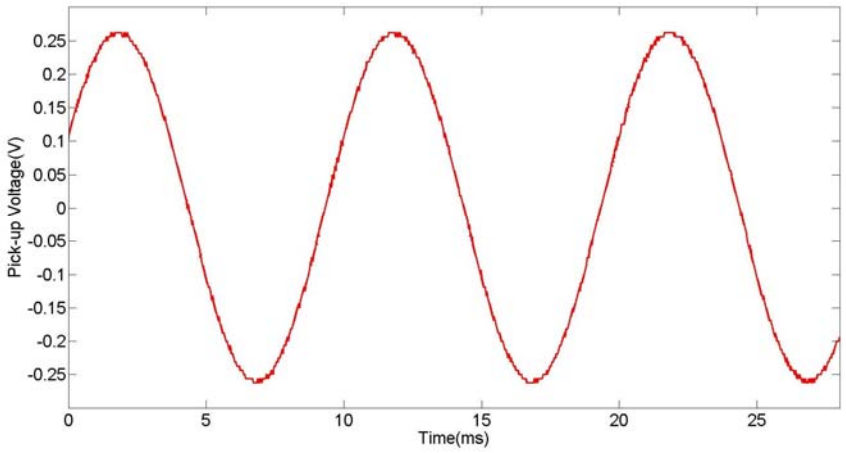
Figure 2.37 Measured frequency response of pick-up low noise amplifiers

Due to its 195 kHz bandwidth, the wideband noise is not attenuated as shown in Figure 2.38 (a).



(a)

Figure 2.38 100 Hz amplified pick-up voltage without(a) low-pass filter



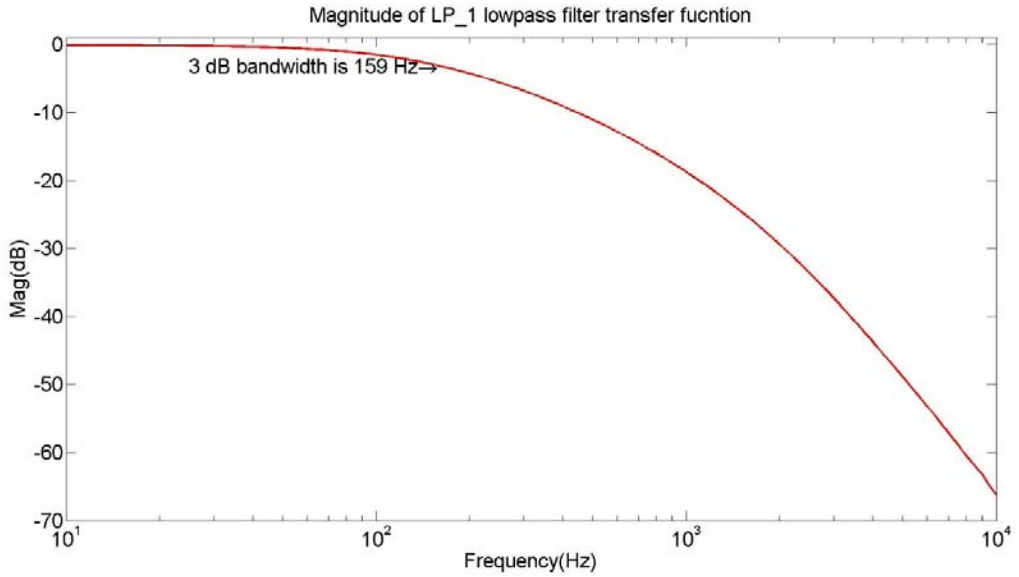
(b)

Figure 2.38 (continued) and with (b) low-pass filter

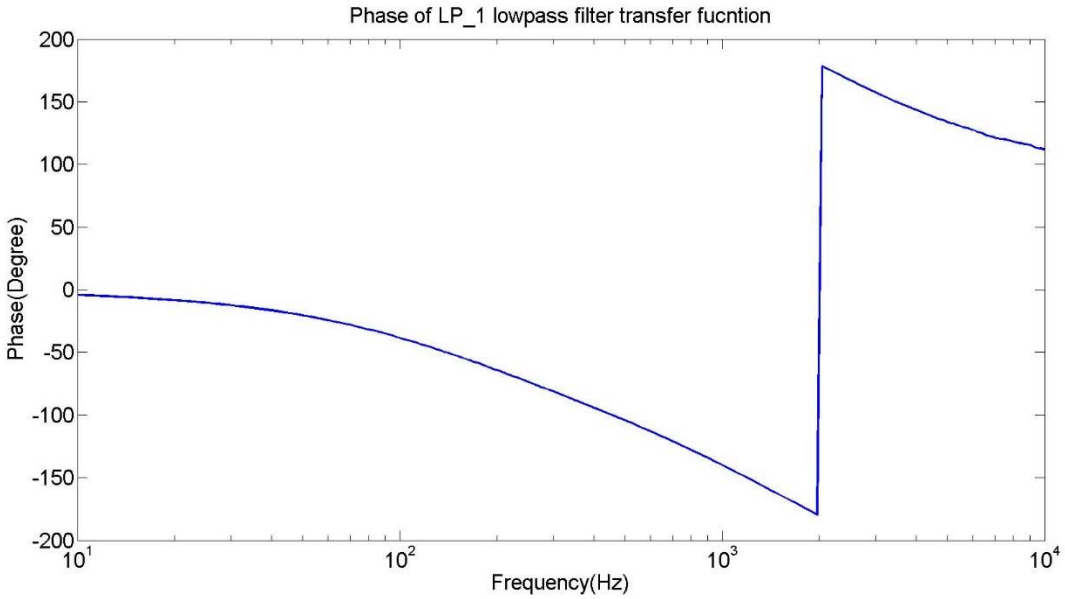
APS1006 system covers a very broad range of frequencies, and therefore it is impossible to use one filter to handle all situations. Item No.18 in Table 2.1 is a filter bank composed of three unity gain low-pass filters. Table 2.4 lists the properties of those three low-pass filters. The low-pass filter bank is followed by an analog 4:1 multiplexer which selects appropriate filter depending on measurement frequency. Figure 2.39-2.41 are the measured filter transfer functions.

Table 2.4 Properties of low-pass filter bank

Designation	Frequency band	3 dB Bandwidth	Comment
LP_1	DC-100 Hz	159 Hz	Third order passive RC filter
LP_2	100 Hz-10 kHz	15.0 kHz	Fourth order active RC filter with Bessel response
LP_3	10 kHz-100 kHz	219 kHz	Fourth order active RC filter with Bessel response

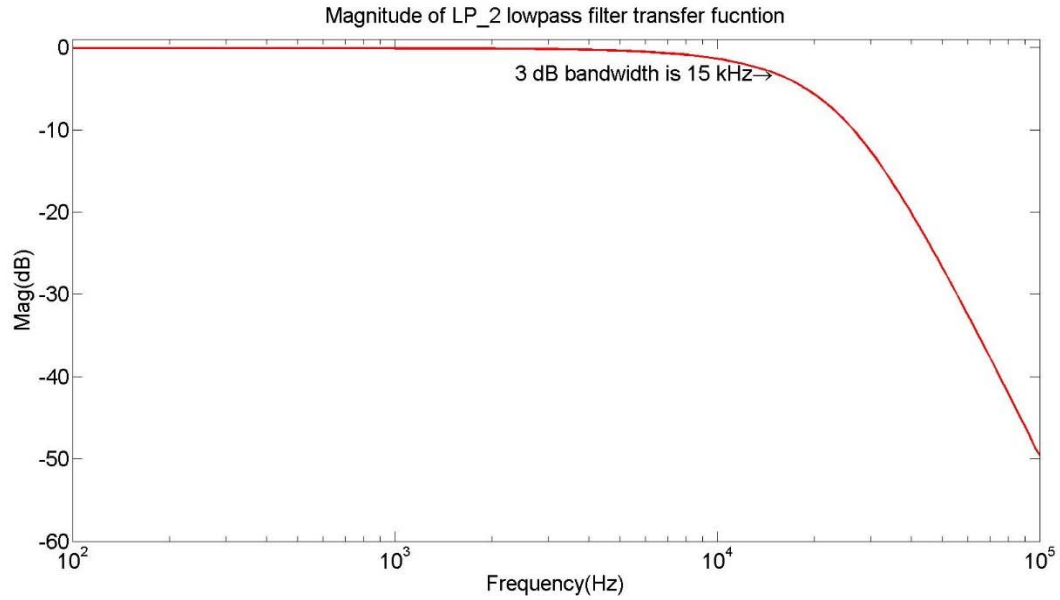


(a)

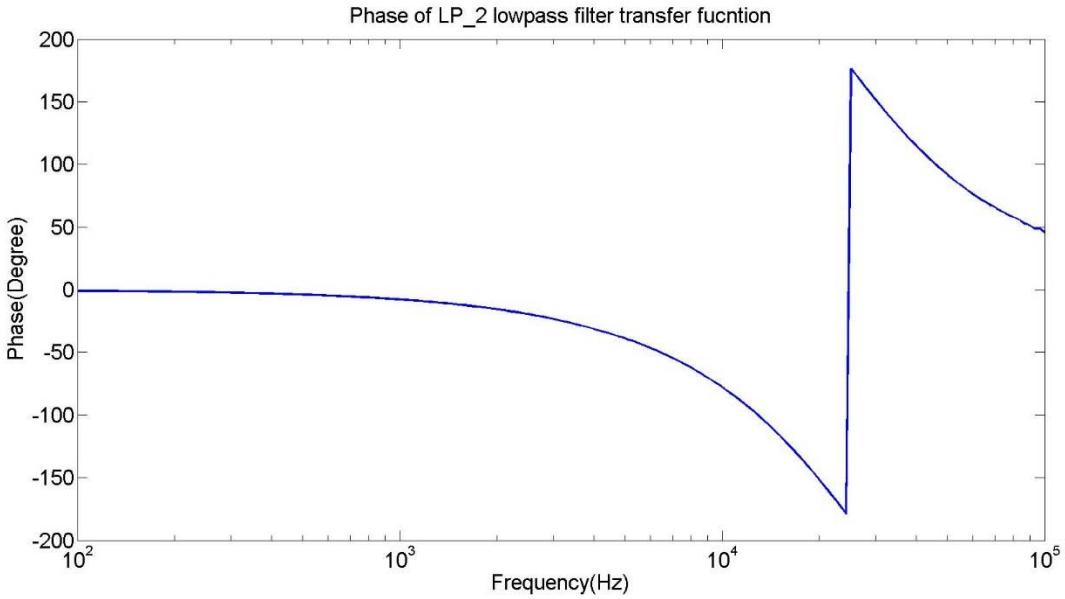


(b)

Figure 2.39 Magnitude (a) and phase (b) of transfer function of LP_1 low-pass filter

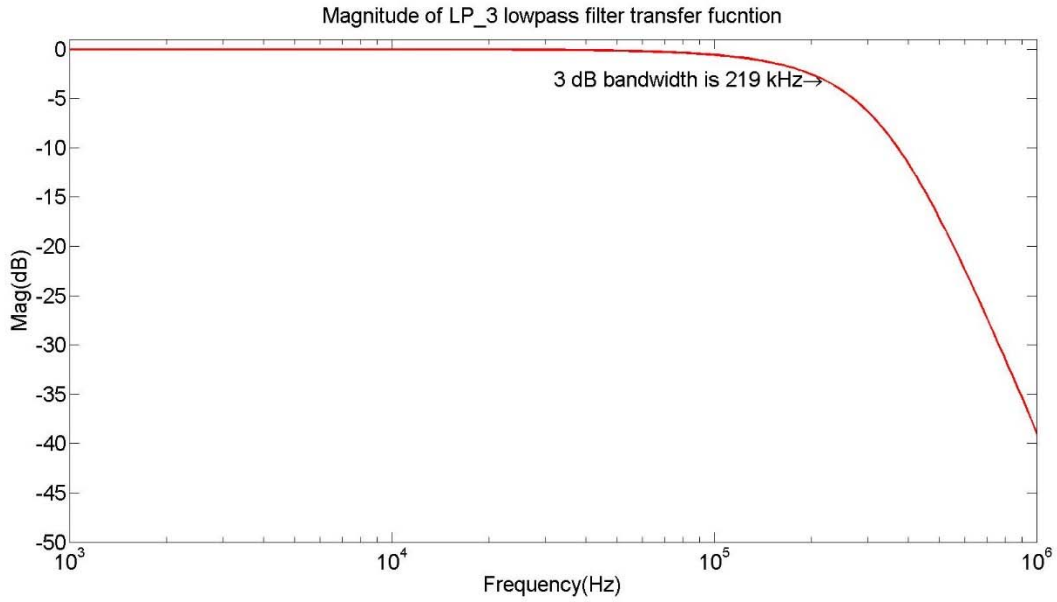


(a)

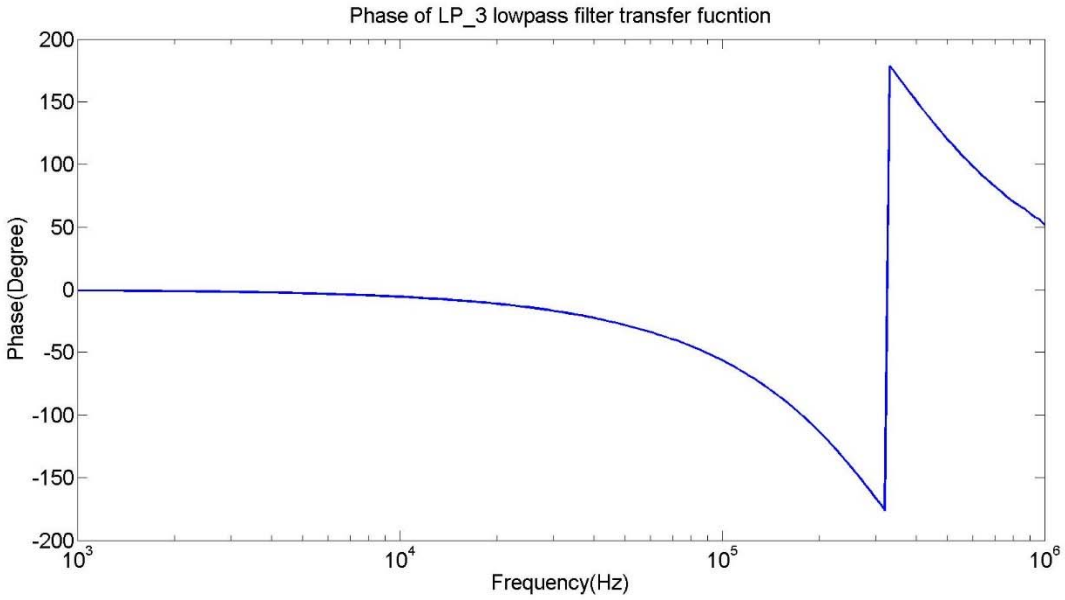


(b)

Figure 2.40 Magnitude (a) and phase (b) of transfer function of LP_2 low-pass filter



(a)



(b)

Figure 2.41 Magnitude (a) and phase (b) of transfer function of LP_3 low-pass filter

Compare Figure 2.38 (a) and (b), LP_1 is very effective at attenuating wide band noise from pick-up amplifiers in frequency band DC to 100 Hz. The same conclusion can be drawn for the other two filters at their respective frequency bands. The design approach of the three filters are not in

the scope of this this dissertation, which is discussed in detail in reference [26]. Even though the design approach is well established, extra consideration must be given to the selection of capacitors in those filters for stability and repeatability concerns. The most commonly used surface mount capacitor is multi-layer ceramic capacitor (MLCC), which is manufactured with a variety of dielectrics .And the most commonly used dielectrics are Z5U, Y5V, X5R and X7R. Unfortunately, the dielectric constant of those material is heavily influenced by applied DC electrical field [27], which causes the capacitance of MLCC changes with applied DC voltage, as shown in Figure 2.42 [28].

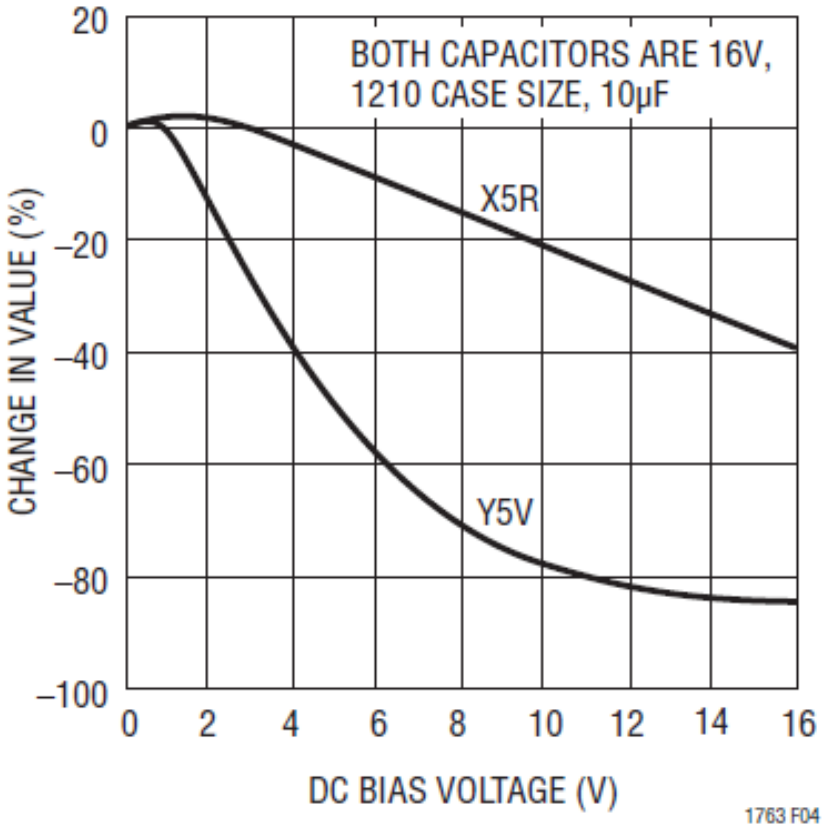


Figure 2.42 MLCC DC bias characteristics

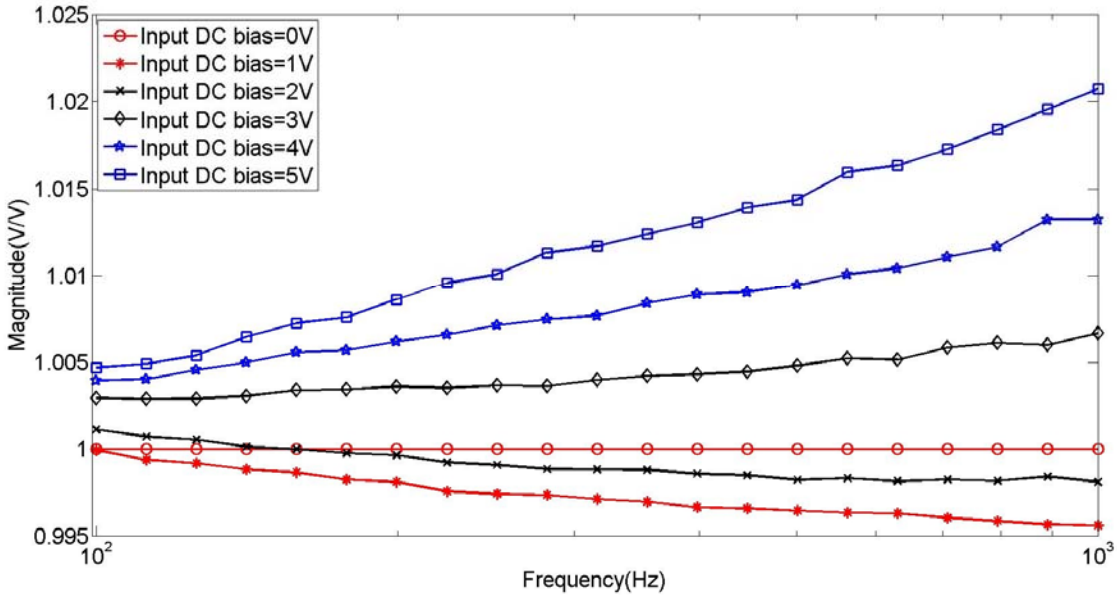


Figure 2.43 Filter transfer function vs. input DC bias (X5R MLCC capacitor)

To verify the performance of filters using MLCC capacitors, an LP_1 filter is assembled using X5R MLCC capacitors and the transfer functions in pass band and stop band are recorded with various input dc bias. Figure 2.43 demonstrates the input bias affects the filter response of this testing filter. Please note that the transfer functions in Figure 2.43 are normalized with respect to 0V dc bias transfer function, thus the red curve with circle is always one. It is also interesting to see that for 1V and 2V bias, the response is below the 0V reference, while for 3V, 4V and 5V bias the response is above the 0V reference. For a third order passive RC filter, this tells that the effective capacitance of those MLCC capacitors at 1V and 2V is higher than 0V normal value, while for 3V, 4V and 5V bias, the capacitance is lower than the normal value. The X5R curve in Figure 2.42 tells that this observation is no coincidence. MLCC's dc voltage dependence makes it not usable for precision filtering application. Also note that MLCC is piezoelectric, thus mechanical stress exerted on the circuit board changes the response of this MLCC filter as well.The

solution to this problem is to use polyphenylene sulfide (PPS) film capacitors, which have no dc voltage dependence and many other advantages compared with MLCC, shown in Figure 2.44 [29].

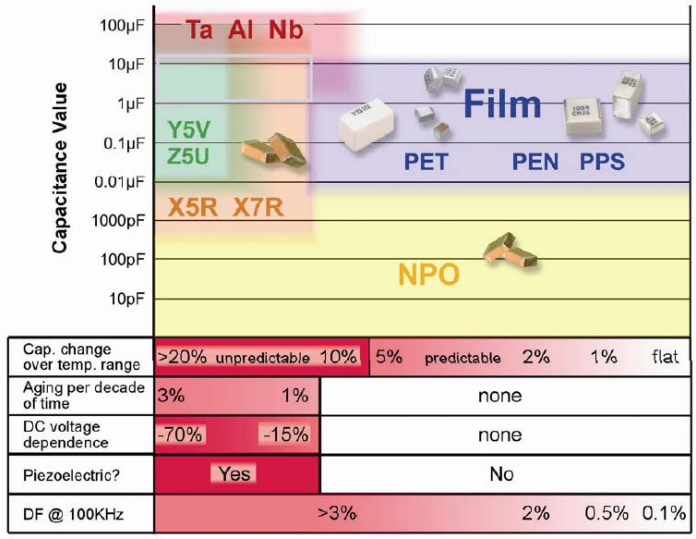


Figure 2.44 Comparison of surface mount capacitors

The LP_1 low-pass filter used in APS1006 uses 10 nF PPS film capacitors. Figure 2.45 shows the test results of this PPS low-pass filter.

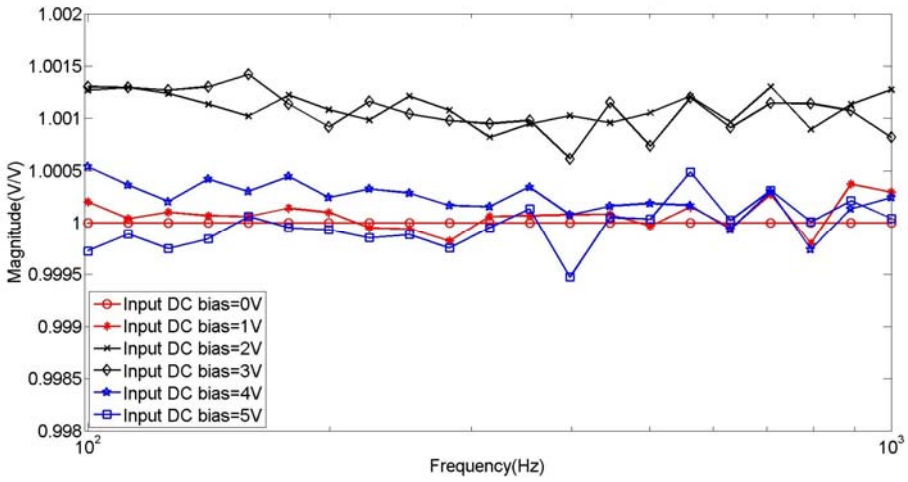


Figure 2.45 Filter transfer function vs. input DC bias (PPS film capacitor)

Figure 2.45 demonstrates that the PPS film based low-pass filter has much smaller dc voltage dependence than MLCC based low-pass filter.

2.2.8 Switched-capacitor band-pass filter

As mentioned in section 2.2.2, one of the approaches to improve measurement speed is to use multi-tone drive current. For example, multi-tone drive voltage in Figure 2.19 allows the transconductance amplifier to generate drive current with up to eight frequency components, which means that the system is able to process these eight frequencies simultaneously. But for the pick-up side, it is very important to separate these eight frequencies before ADC for dynamic range and noise concerns. This requires an eight channel programmable band-pass filter bank. Conventional continues time band-pass filter is not suited due to lack of programmability. Switched-capacitor bandpass filter is well suited in this case, because the center frequency can be programmed by an input clock. MAX7490 dual universal switched-capacitor filter is used to build this eight channel programmable filter bank. Detailed design approach can be found in reference [30]. Clock input to center frequency ratio is 100:1. Take schematic in Figure 2.46 for an example, a 10 kHz filter clock input make this circuit act as a fourth order bandpass filter centered at 100 Hz. Figure 2.47 demonstrates the programmability of the switched-capacitor bandpass filter.

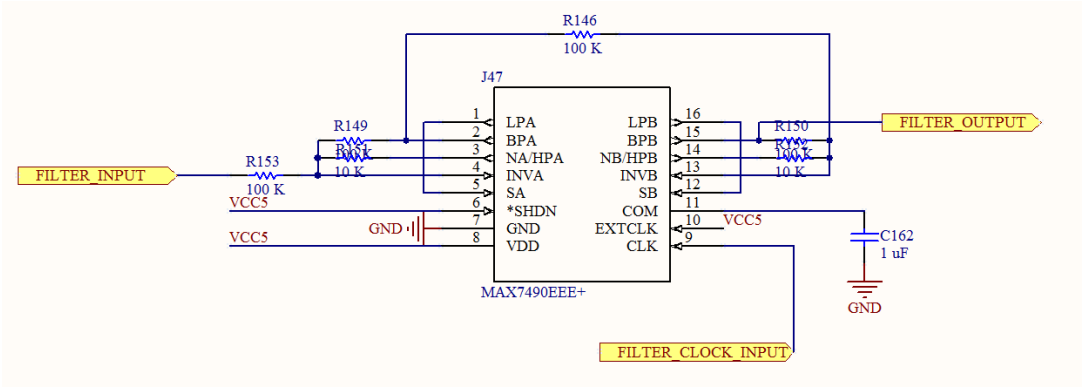
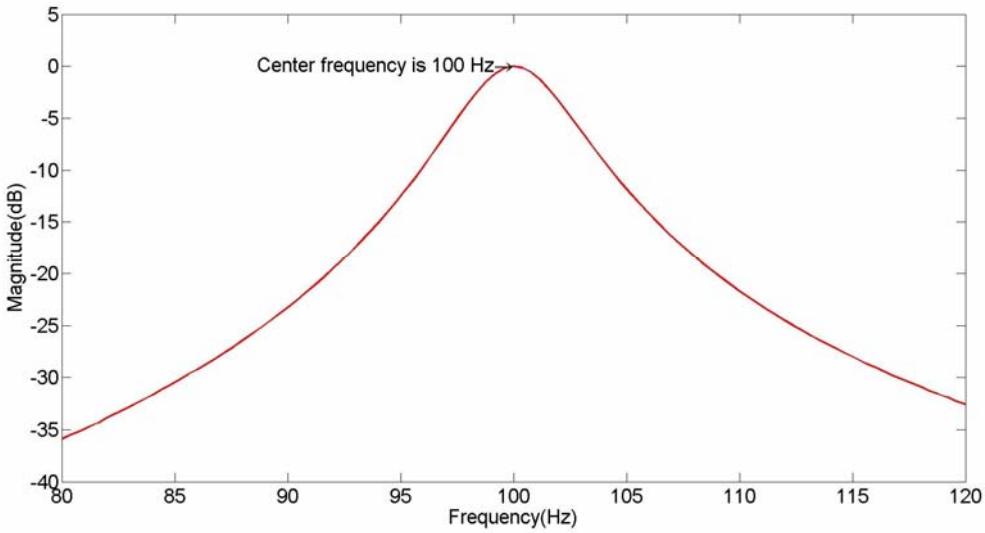
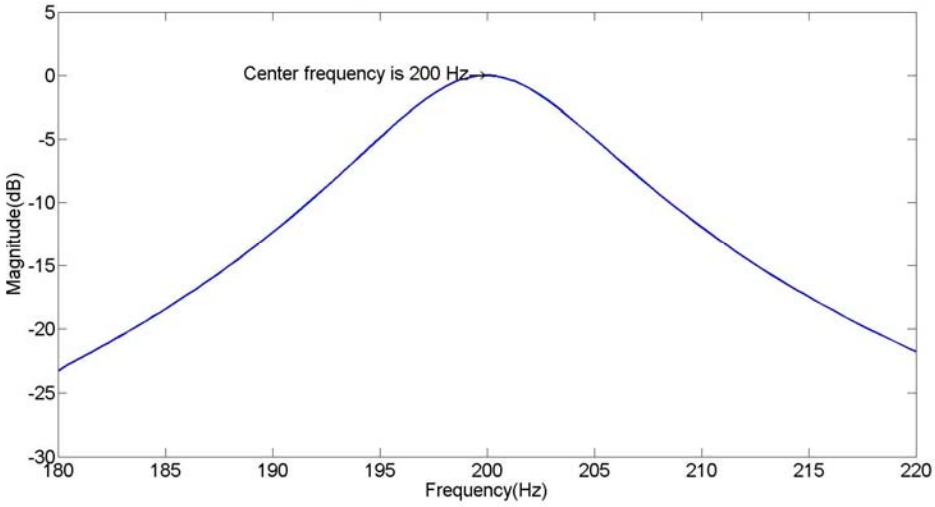


Figure 2.46 Simplified schematic of programmable band-pass filter (one channel)



(a)



(b)

Figure 2.47 Measured band-pass filter frequency response with 10 kHz clock (a) and 20 kHz clock (b)

2.2.9 Analog to digital converter

True bipolar input ADC LTC2328-16 is used in this application. LTC2328-16 is a low noise, high speed 16-bit successive approximation register ADC. It achieves ± 1.5 LSB INL and no missing codes at 16 bits with 93.5 dB SNR [31]. Because of its true bipolar input, the amplified voltage can be directly feed to the input port of this ADC without using level shifter.

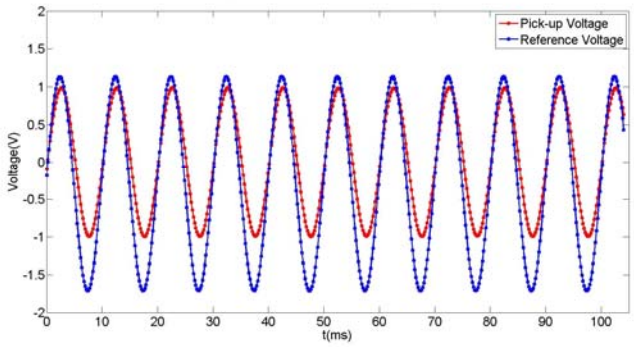
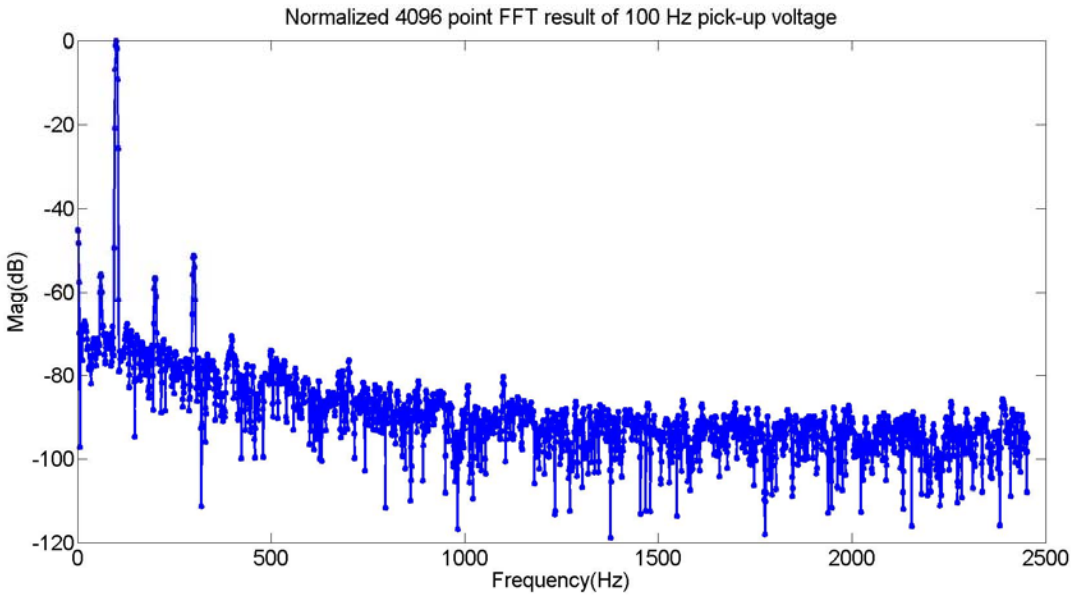
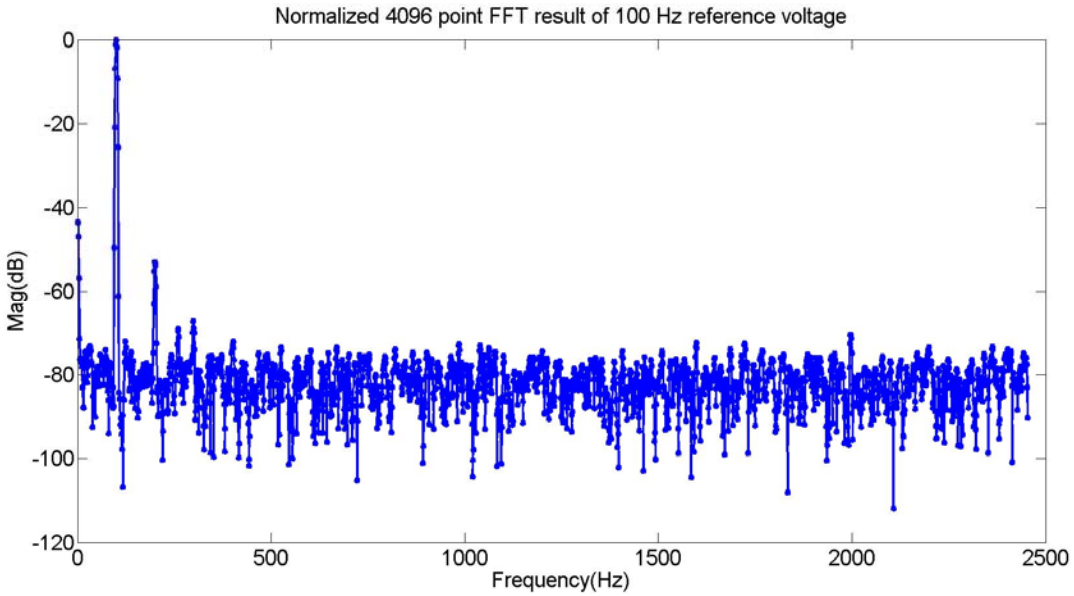


Figure 2.48 Reference and pick-up voltage captured by LTC2328-16 ADC in time domain



(a)

Figure 2.49 4096 point FFT of the 100 Hz pick-up waveform (a)



(b)

Figure 2.49 (continued) 4096 point FFT of the 100 Hz reference waveform (b)

2.2.10 Low noise amplifier for pick-up voltage

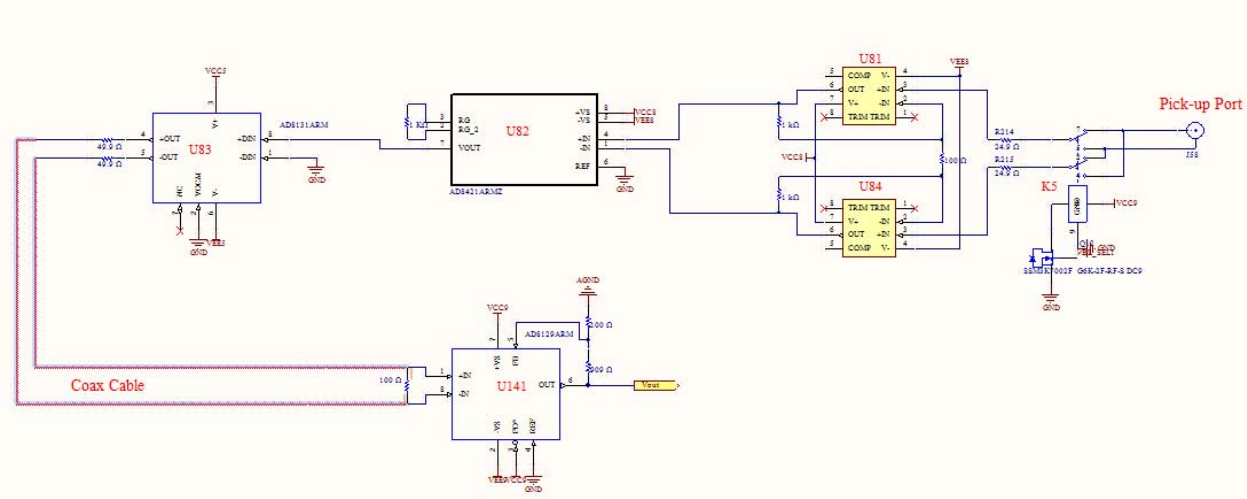


Figure 2.50 Schematic of pick-up four stage amplifier

The circuit shown above has four stages, providing total gain of 66.5 dB as shown in Figure 2.37. The noise performance is determined by the first stage preamplifier in Figure 2.51

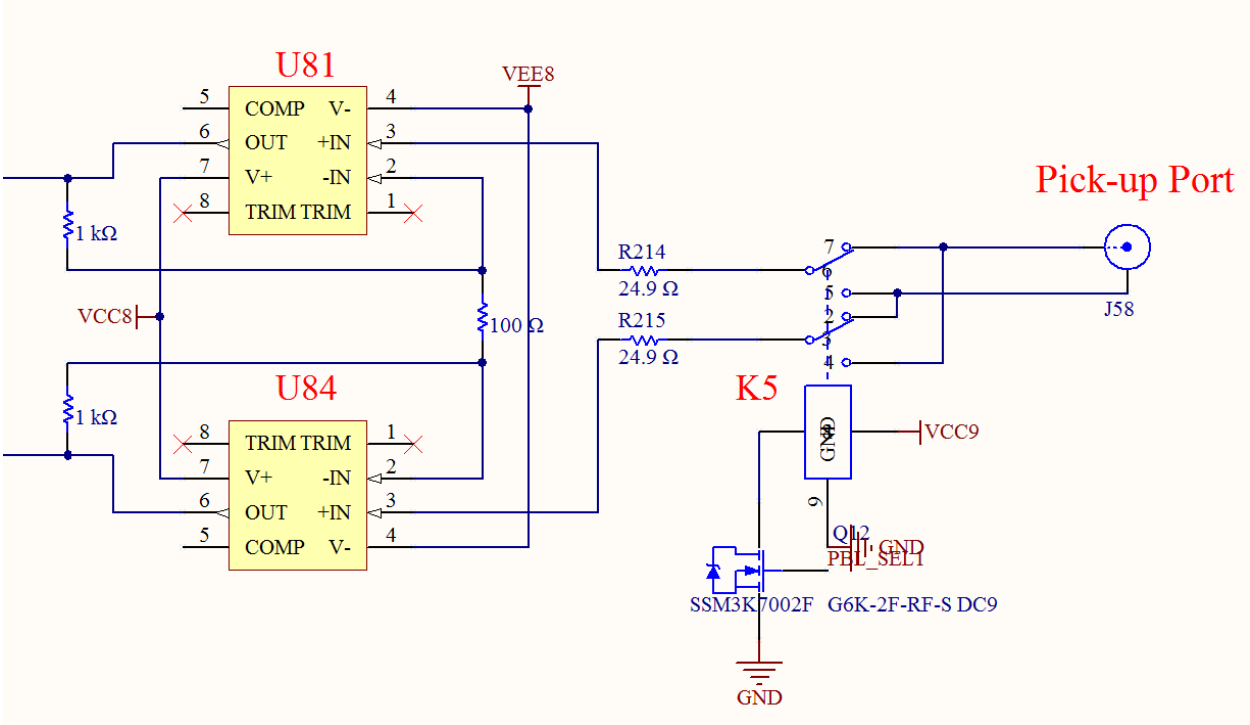


Figure 2.51 Schematic of first stage low noise preamplifier

K5 is a DPDT relay for common mode cancellation. Since it is a mechanical relay and the insertion resistance is minimal, it will not introduce measureable noise. U81 and U84 are identical ultra-low noise operational amplifier LME49990, which has input voltage noise density as low as $0.88\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ [32]. With 43 Hz $1/f$ corner frequency [32], LME49990 is well suited for demanding ACPD applications, which require low noise at low frequency range.

This preamplifier is configured as a high input impedance differential buffer with a gain of 21, which means that its input referred noise approximately equals to the overall input referred noise of the four stage amplifier.

The total input referred noise of the preamplifier can be calculated by

$$e_t = \sqrt{2(e_n^2 + r_n^2 + (I_n R_{\mathrm{eq}})^2)} \qquad (2.2)$$

R_{eq} is the total equivalent source resistance

r_n^2 is the thermal noise from sources resistance

e_n is the input voltage noise density

I_n is the input current noise density

$$R_{\text{eq}} = \frac{1000 * 50}{1000 + 50} + 24.9 = 72.5\ \Omega$$

$$r_n = 1.12\ \text{nV}/\sqrt{\text{Hz}}$$

$$e_n = 0.88\ \text{nV}/\sqrt{\text{Hz}}$$

$$I_n = 2.8\ pA/\sqrt{\text{Hz}}$$

Use expression 2.2 and noise specifications from [32], the input referred noise density of this preamplifier is $2.034\ \text{nV}/\sqrt{\text{Hz}}$ when frequency is well above corner frequency. To verify this calculated result, the output noise power spectrum of this four stage amplifiers (inputs shorted) is measured by a low frequency spectrum analyzer.

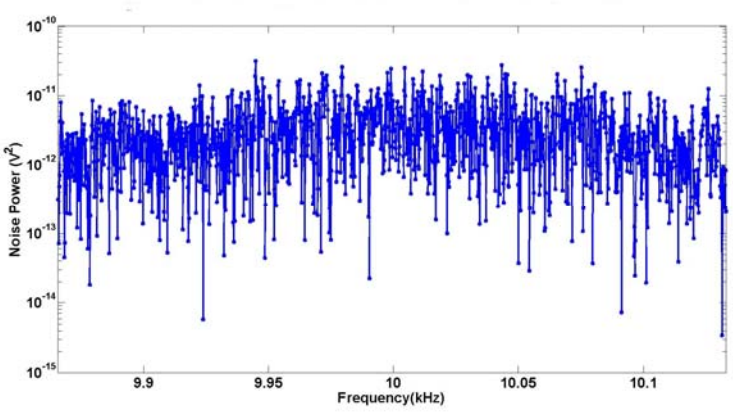


Figure 2.52 Measured output noise power spectrum of four stage amplifier centered around 10 kHz

From the power spectrum in Figure 2.52, the measured output referred noise density is $4.3\ \text{uV}/\sqrt{\text{Hz}}$. Dividing output noise density by 66.5 dB gain yields $2.036\ \text{nV}/\sqrt{\text{Hz}}$ input referred noise density, which agrees with previous calculation $2.034\ \text{nV}/\sqrt{\text{Hz}}$. Please note that this

calculation is only valid for frequency higher than corner frequency. For frequency lower than corner frequency, 1/f noise dominates the noise density as shown in Figure 2.53.

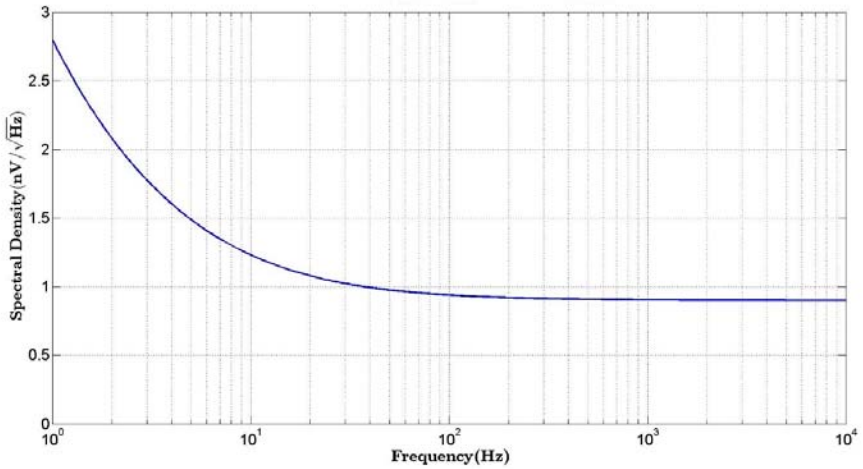


Figure 2.53 Noise spectral density of LME49990 amplifier [32]

Since it has been verified that the calculation based on data point at 10 kHz of Figure 2.53 agrees with measurement results at the same frequency, the same calculation can be applied to other frequencies:

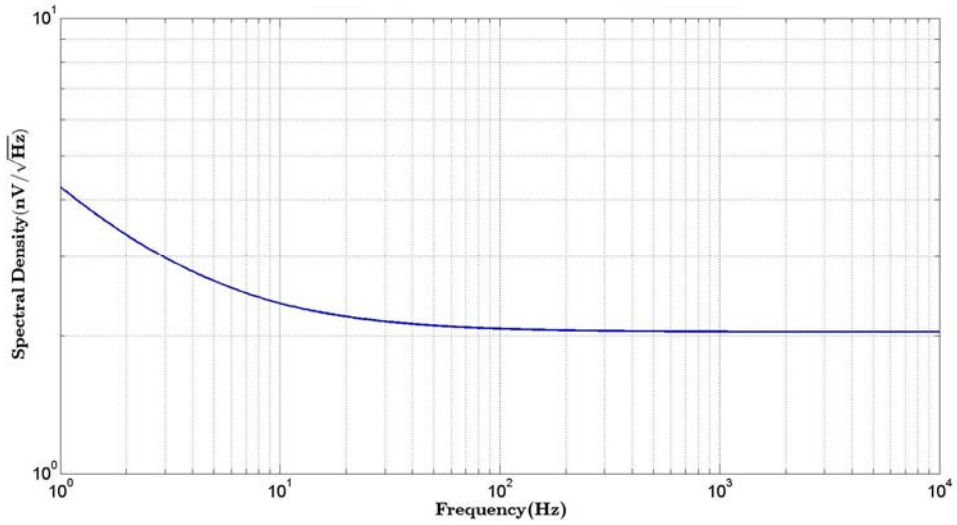


Figure 2.54 Input referred noise spectral density of four stage amplifier

Curve in Figure 2.54 has the following expression:

$$e_t = \sqrt{2(\frac{2.65^2}{f} + 0.88^2 + 0.14^2 + 1.12^2)}\ \text{nV}/\sqrt{\text{Hz}} \qquad (2.3)$$

Expression 2.3 is the input referred noise spectral density of four stage amplifier, including 1/f noise and white noise. One way to validate expression 2.3 is to observe the noise voltage in time domain. In this experiment, fourth order low pass filter LP_2 in Table 2.3 is used as anti-aliasing filter. LP_2 has a 3 dB bandwidth of 15 kHz, thus its equivalent noise bandwidth is 15.375 kHz. The input referred R.M.S noise in time domain can be calculated by

$$N_{in,\text{rms}} = \sqrt{\int_1^{15375} 2(\frac{2.65^2}{f} + 0.88^2 + 0.14^2 + 1.12^2)\, df} = 251\ nV \qquad (2.4)$$

An additional gain of 35.5 dB is added to the signal chain so that the output noise amplitude is large enough for oscilloscope to capture. The total gain is 102 dB, which yields a theoretical output referred R.M.S noise of 31.82 mV.

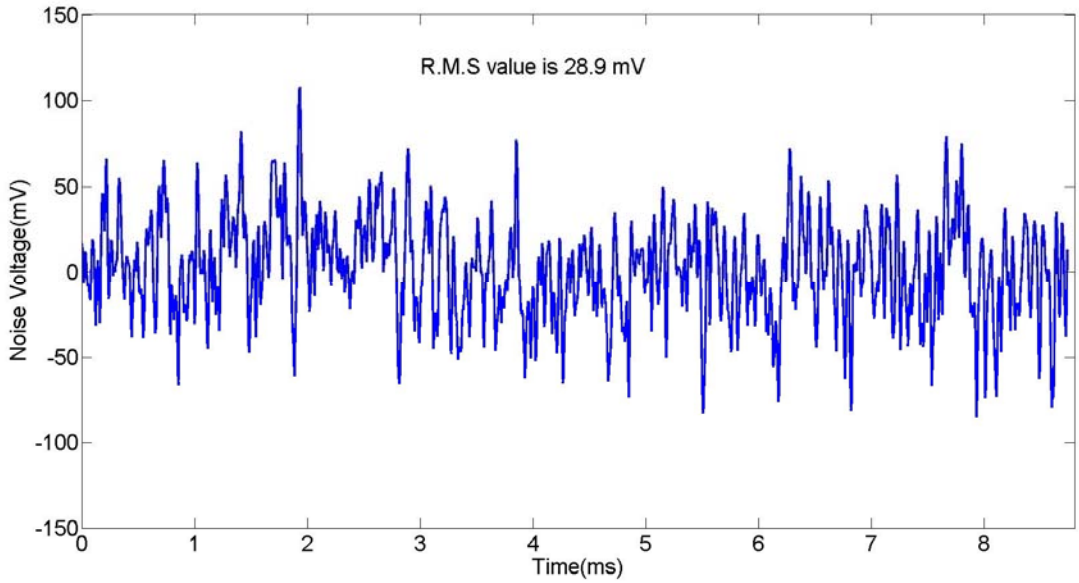


Figure 2.55 Output noise captured by oscilloscope in time domain

The measured output noise's R.M.S value is 28.9 mV, which is close to theoretical calculation 31.82 mV, validating expression 2.3. In comparison, the noise performance is better than Stanford Research Systems SR830, which has a typical input noise density of 6 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz [10]. Comparing Figure 2.54 and Figure 2.56, it can be concluded that the noise performance this four

stage amplifier is also better than some of the newly developed lock-in amplifiers, such as MFLI Lock-in Amplifier from Zurich Instruments [33].

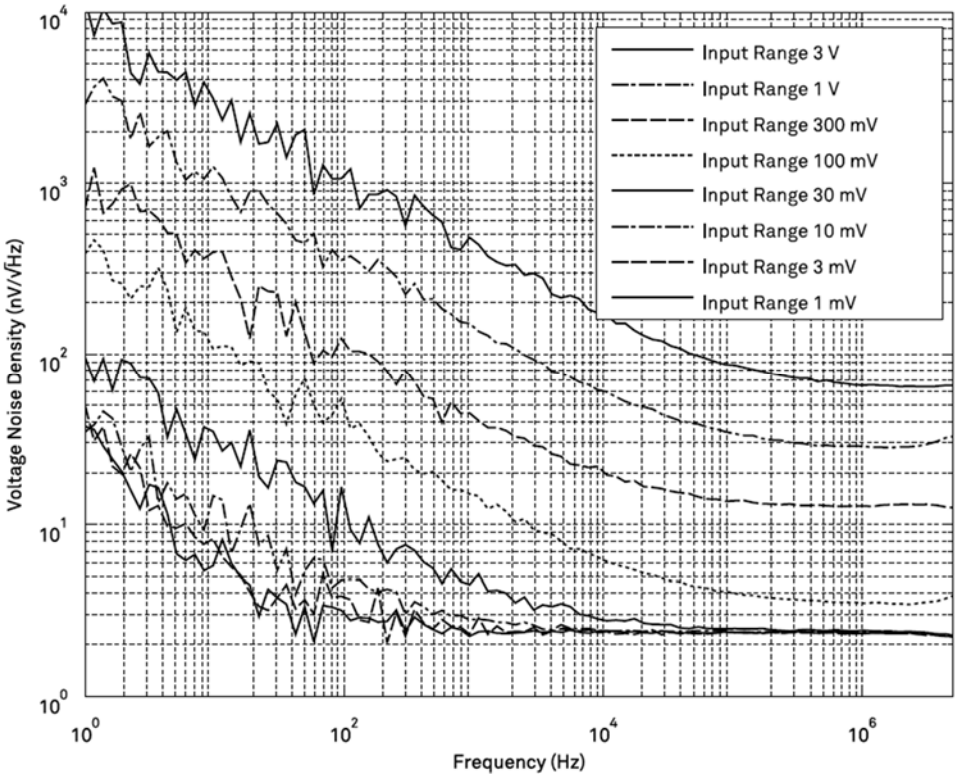


Figure 2.56 Input referred noise spectral density of MFLI Lock-in Amplifier [33]

2.3 Conclusion

APS1006 is an integrated ACPD measurement system that covers frequency from DC to 100 kHz. It contains onboard lock-in amplifier, voltage signal generator, transconductance amplifiers, and low noise amplifiers. APS1006's hardware is designed for optimum performance. Low noise, high current dc-dc power regulators generate high quality dc supply voltage for following transconductance amplifiers. Combining high current transconductance amplifiers and wide bandwidth transconductance amplifiers allows the system cover wider frequency range. High dynamic range multi-tone DDS signal generator gives the system sufficient flexibility for different modes operation. Continues time low pass filter bank attenuates wideband noise when the system

in single tone mode. Programmable switched-capacitor bandpass bank is dedicated for multi-tone mode, in which up to eight frequencies can be measured simultaneously. The noise performance of pick-up side amplifiers is better than some of widely used commercially available lock-in amplifiers. This chapter covers the design and test of most important parts of the hardware, but the actual performance depends on the signal processing method which is discussed in next chapter.

CHAPTER 3. SIGNAL PROCESSING AND CALIBRATION

3.1 Overview

Chapter 2 discusses about hardware design and test, which lays down a sound foundation for optimum measurement performance. The way firmware process the captured time domain data significantly affect the system performance for a given hardware. The goal is to improve measurement speed without sacrificing measurement reliability and repeatability. Since the final output of APS1006 is normalized pick-up voltage, the system must acquire information regarding pick-up voltage and drive current simultaneously. As shown in Figure 2.2, the reference voltage contains information of drive current, while amplified pick-up voltage contains information of pick-up voltage. Thus, the relationship between reference voltage and drive current, as well as the relationship between amplified pick-up voltage and pick-up voltage must be known prior to measurement. Those relationships can be determined by calibration process. Normalized pick-up voltage can then be calculated by merging measured raw data and calibration data. Since APS1006 is working at specific frequency, the raw data is a phasor at measurement frequency. Converting captured time domain waveform to phasor is the most important task of the system firmware. APS1006 is a general purpose system, thus it has to be compatible with a variety of materials with vastly different conductivity and permeability. APS1006's internal gain and drive strength has to be automatically adjusted per sample under test.

3.2 Time Domain to Frequency Domain Conversion

3.2.1 Single tone fast Fourier transform

Fast Fourier transform (FFT) is a convenient tool to convert time domain waveform into a phasor. The implementation of this algorithm is well established and in Matlab it only involves one command. However, in this particular application, the FFT algorithm must be executed on an 80 MHz 32-bit fixed point microcontroller PIC32MX795F512L, which has 128 KB ram and 512 KB flash [34]. The reason for this arrangement is that, for 4096 points of data for both pick-up voltage and reference voltage, it takes too long to transfer them to PC. For the 1115200 baud rate serial port, data transfer takes at least 1.28 seconds. For a typical 31 frequencies scan, the total data transfer time would be 1.28*2*31=79.36 seconds, which is unacceptable. Thus FFT must be handled locally on the board. As the name might suggests, microcontroller PIC32MX795F512L is not a particularly powerful processor. It only has 124.8 DMIPS performance at 80 MHz [34], and lacking a hardened float point co-processor makes it difficult to implement floating point FFT algorithm on this processor. Figure 3.1 [35] gives DMIPs performance of commonly used hard and soft processors. Clearly, PIC32MX795F512L is chosen in APS1006 not because of its performance but its ease of use from both software and hardware perspective. For fully commercialized version of this system, more powerful SOC, such as XC7Z030 or digital signal processor (DSP), such as TMS320C6657 [36] should be used. Table 3.1 gives suggested hardware platform for future development.

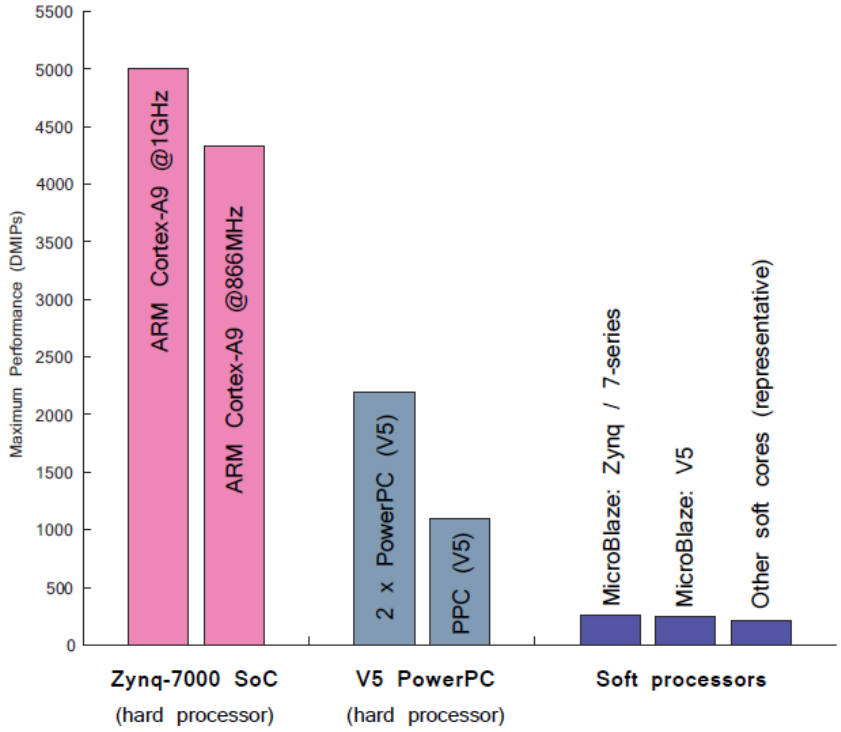


Figure 3.1 Performance comparison of hard and soft processors

Table 3.1 Suggested hardware platform

Part Number	Type	Main Clock Speed	Comment
XC7A15T and TM4C1294NCZAD	FPGA-Processor Combination	120 MHz	Low cost Artix 7 FPGA and ARM M4 processor
XC7A50T and TMS320C6748	FPGA-DSP Combination	375 MHz	Low cost Artix 7 FPGA and low-end floating point DSP
XC7K70T and TMS320C6657	FPGA-DSP Combination	800 MHz	Mid-range FPGA and mid-range floating point DSP
XC7K70T and AM5728	FPGA-AP Combination	1500 MHz	Mid-range FPGA and high end application processor
XC7Z100	FPGA-AP SOC	1000 MHz	All-programmable System-on Chip (SOC) [37]

In APS1006, slow but easy to use PIC32MX795F512L is our main processor, thus when developing FFT routines in this platform, we must refrain from using floating point algorithm. A 32 bit fixed-point routine is developed for this application, which computes the complex Fast Fourier Transform of the input sequence, and the output can be expressed as

$$\text{output}[n] = \frac{1}{2^{\log 2(N)}} \sum_{k=0}^{N-1} \text{din}[n] \times e^{-j \times \frac{2\pi kn}{N}} \tag{3.1}$$

For a 4096 point FFT, this routine takes 12 ms to complete.

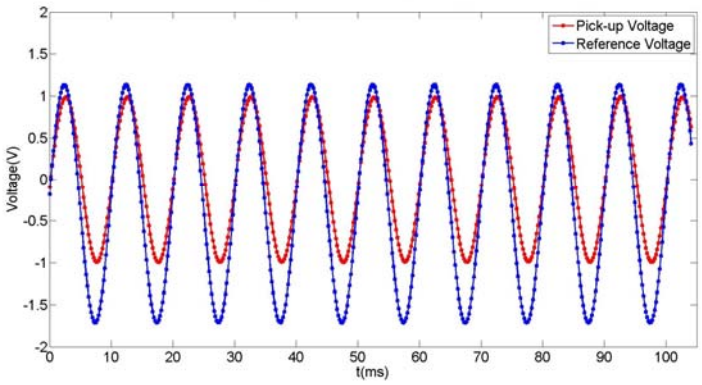
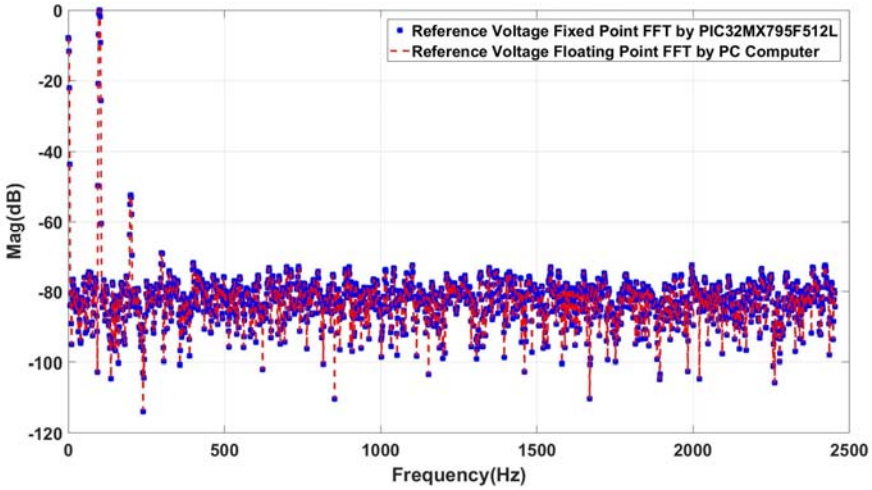
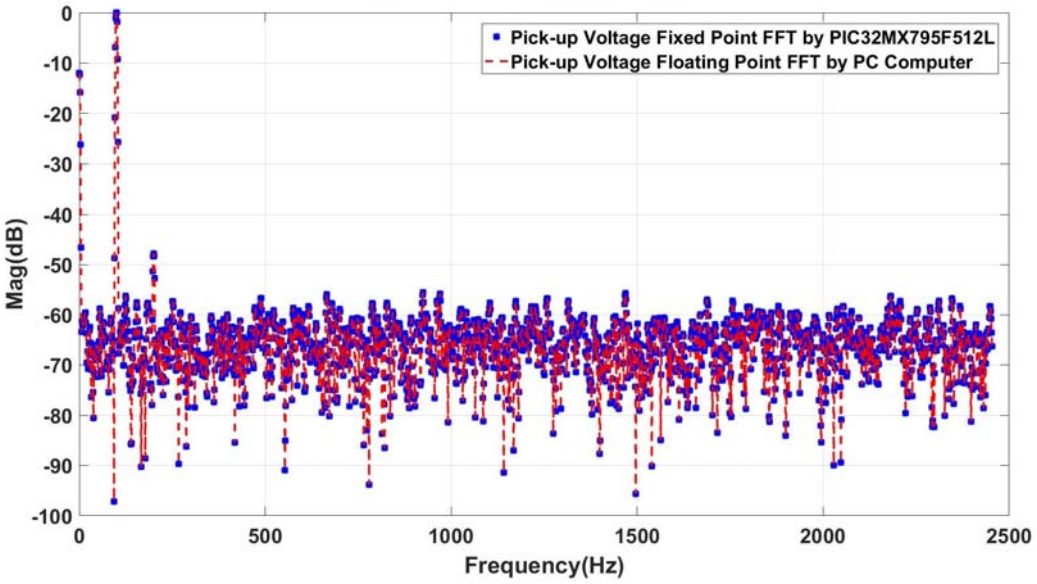


Figure 3.2 FFT routine input data in time domain (100 Hz)



(a)

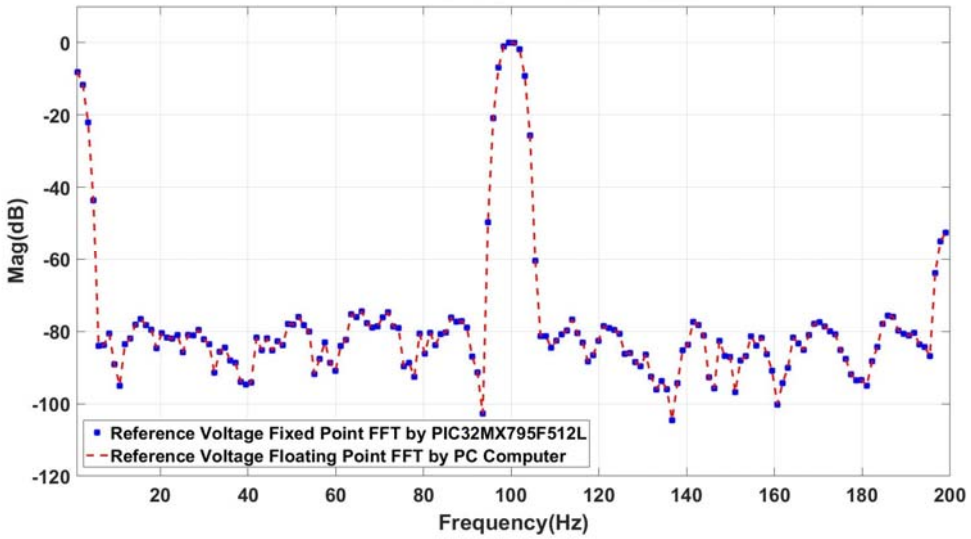
Figure 3.3 FFT results comparison for (a) reference voltage



(b)

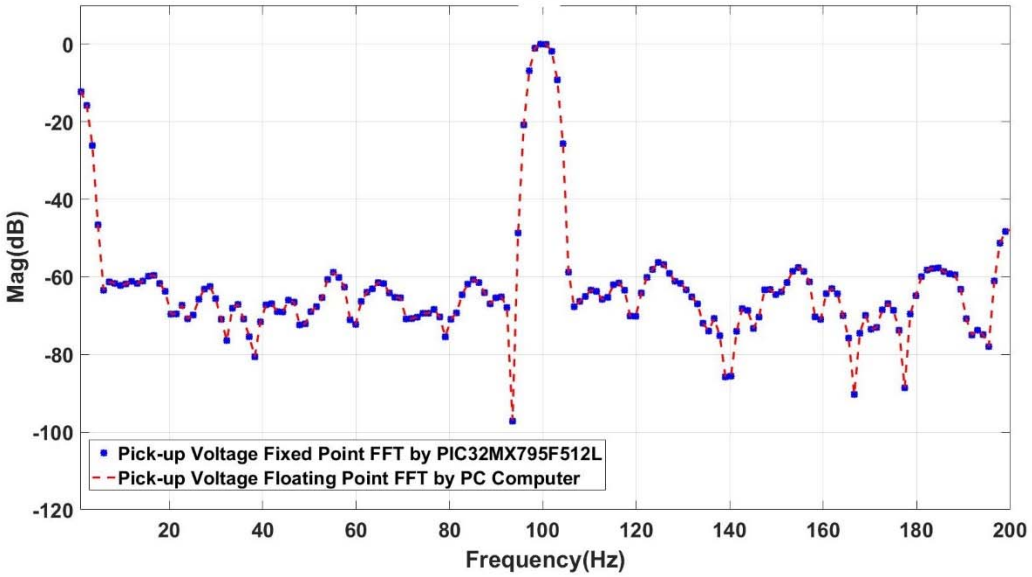
Figure 3.3(continued) and for (b) pick-up voltage

Please note that the noise ground of pick-up voltage is higher than that of reference voltage. Figure 3.4 gives a zoomed view of those two sets of FFT results.



(a)

Figure 3.4 FFT results comparison for (a) reference voltage



(b)

Figure 3.4(continued) and for (b) pick-up voltage

Table 3.2 lists the ratio between pick-up voltage and reference voltage for both cases:

Table 3.2 Ratio between pick-up and reference

FFT Arithmetic	Mag	Phase
Floating Point	0.638642	27.371277 degree
32-Bit Fixed Point	0.638651	27.370605 degree

Figure 3.4 and Table 3.2 have demonstrated that fixed point FFT calculation by PIC32MX795F512L is very accurate. However, despite its accuracy, single tone FFT is not the ideal method in terms of measurement speed. For some applications, ACPD measurement starts at 1 Hz, and samples up to 10 points from 1 Hz to 10 Hz. In order to make FFT result accurate, system must sample at least 7 periods of the frequency under test. Data accusation of 1 Hz signal takes up to 7 seconds to complete, if you take into consider of common mode cancellation by

toggling input polarity, 1 Hz alone will cost about 14 seconds. The first decade (1 Hz to 10 Hz) shall take 41 seconds to finish, which is too long for our design goal.

3.2.2 Multi-tone fast Fourier transform

One of the methods to improve measurement speed is to measure multiple frequency simultaneously. In Chapter Two, we discussed multi-tone DDS signal generator and eight channel programmable switched-capacitor band-pass filter. Combining those two pieces of hardware allows the system to measure up to eight different frequencies at one time, saving tremendous amount of time.

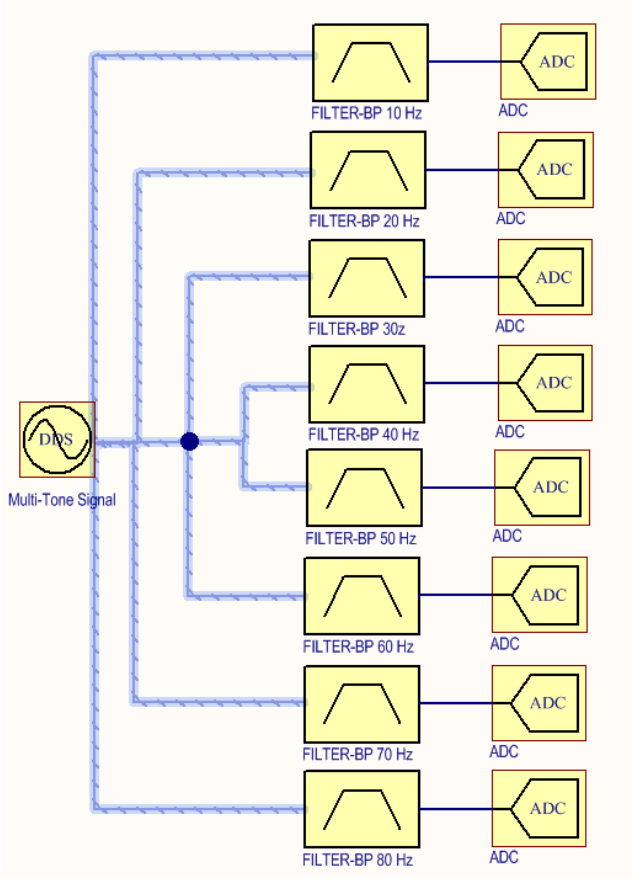
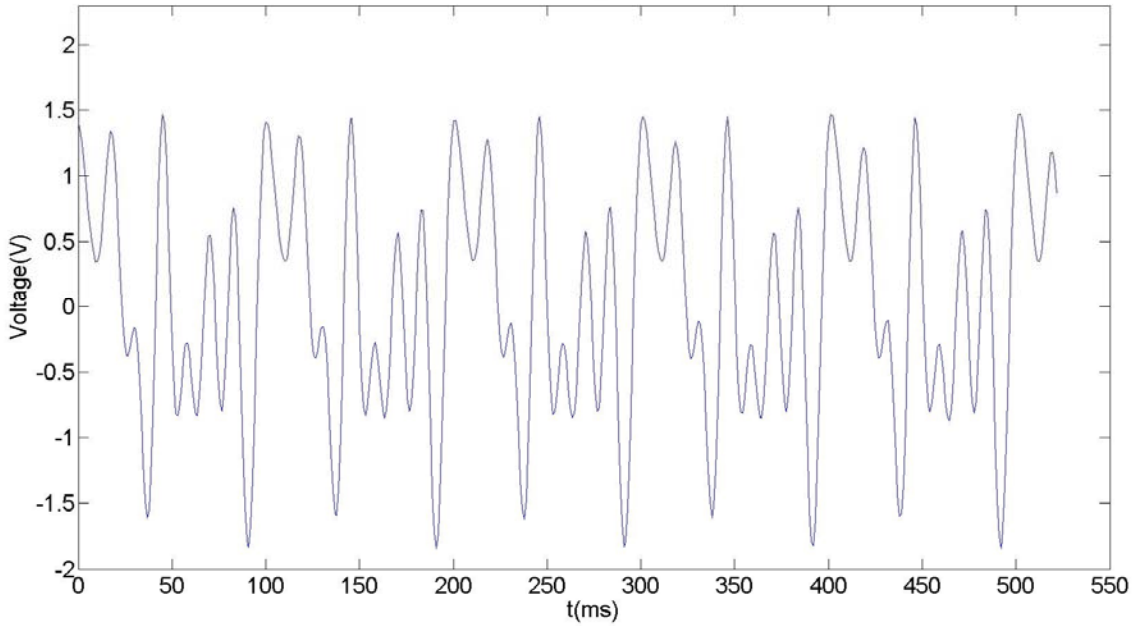
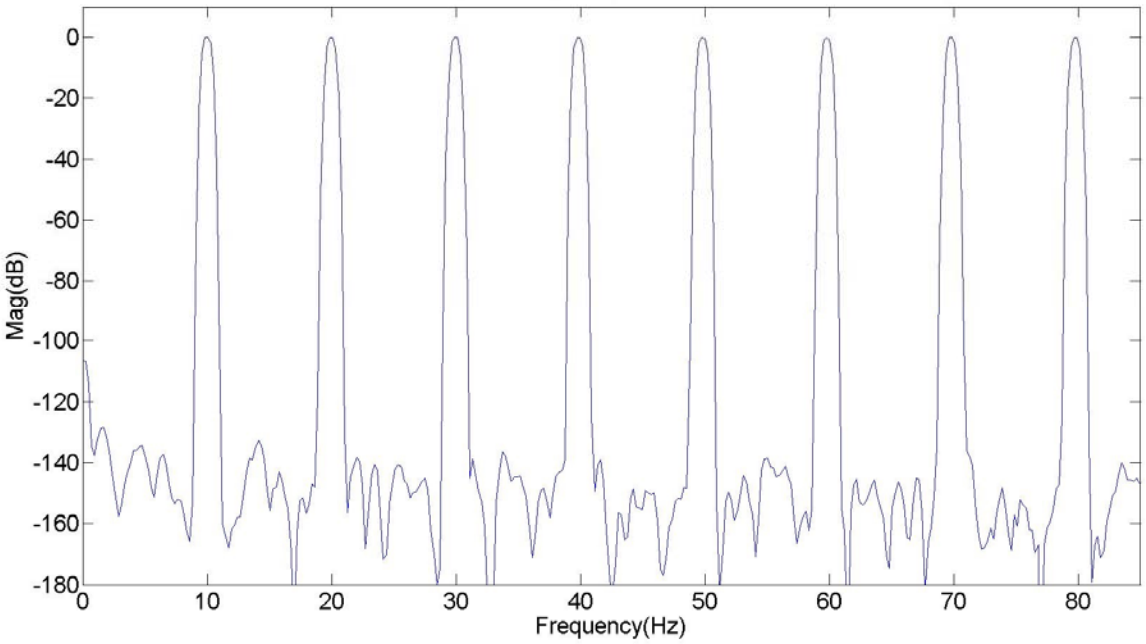


Figure 3.5 Multi-tone measurement scheme diagram



(a)



(b)

Figure 3.6 Multi-tone DDS output in time domain (a) and frequency domain (b).

The multi-tone signal contains eight different frequencies, and the eight channel bandpass filters are programmed to have the same eight center frequencies. Because of the bandpass filter, different frequencies are separated before ADC, improving the dynamic range and accuracy of the system. After digitalization, the sampled signals are processed using the same FFT routine described in previous section. By doing this, for a given decade, the measurement time is determined by the lowest frequency in this decade. For 1 Hz to 10 Hz decade, the data acquisition time will be 14 seconds instead of 41 seconds.

The multi-tone measurement scheme seems to be the perfect choice for this design. However, three major drawbacks prevent it from being used in APS1006. The first drawback is the measurement is still not fast enough. Previous calculation of 14 seconds for 1 Hz to 10 Hz assumes the system only sample 7 periods of 1 Hz signal. But in reality, system will sample up to 14 periods for 1 Hz signal due to signal to noise ratio concerns, which doubles data acquisition time from 14 seconds to 28 seconds. The second drawback is that programmable switched capacitor filter has clock feedthrough problem. The programmable switched capacitor bandpass filter is driven by a clock which defines the center frequency of this bandpass filter. In this design, clock to center frequency ratio is 100:1, which means that 10 kHz clock yields a bandpass filter centered at 100 Hz, as shown in Figure 3.7. Due to unavoidable parasitic capacitance within the chip, part of the clock signal will leak into the output pins, even if no input signal is presented. Figure 3.8 demonstrates this phenomenon, and in Figure 3.8 the input of the bandpass filter is grounded.

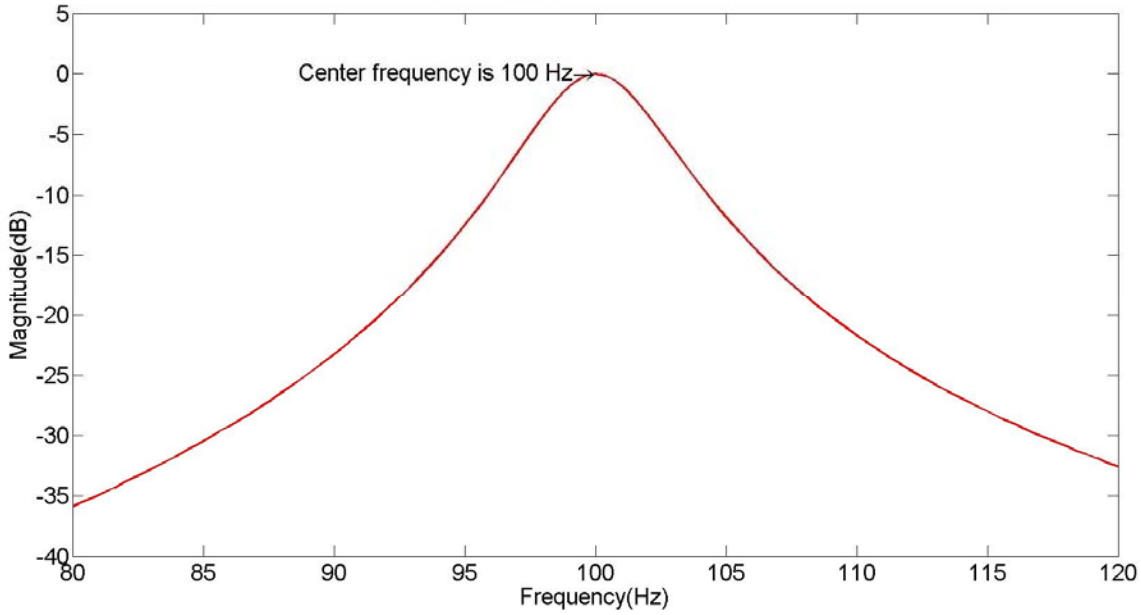


Figure 3.7 Measured transfer function of 100 Hz bandpass switched capacitor filter

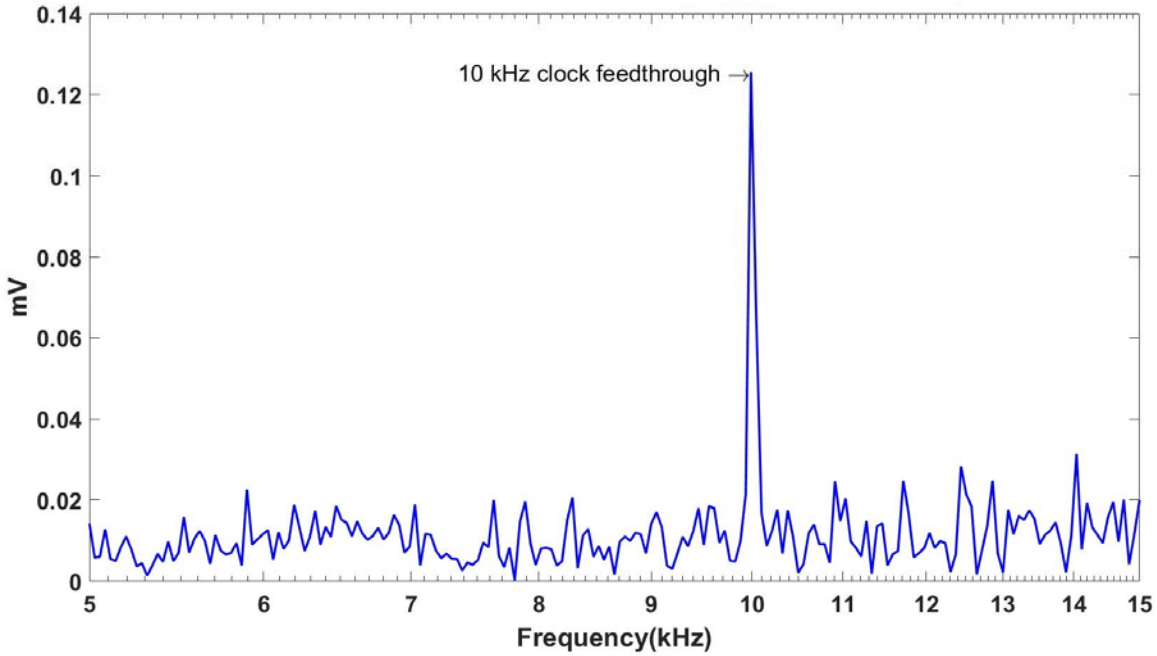
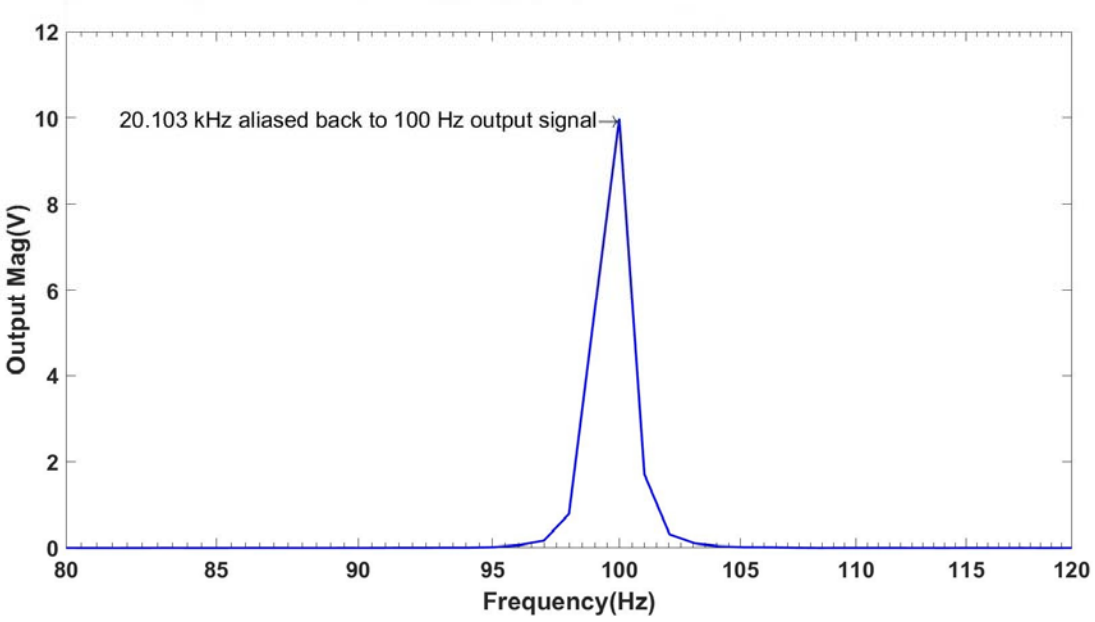


Figure 3.8 Measured 10 kHz clock feedthrough of 100 Hz bandpass switched capacitor filter

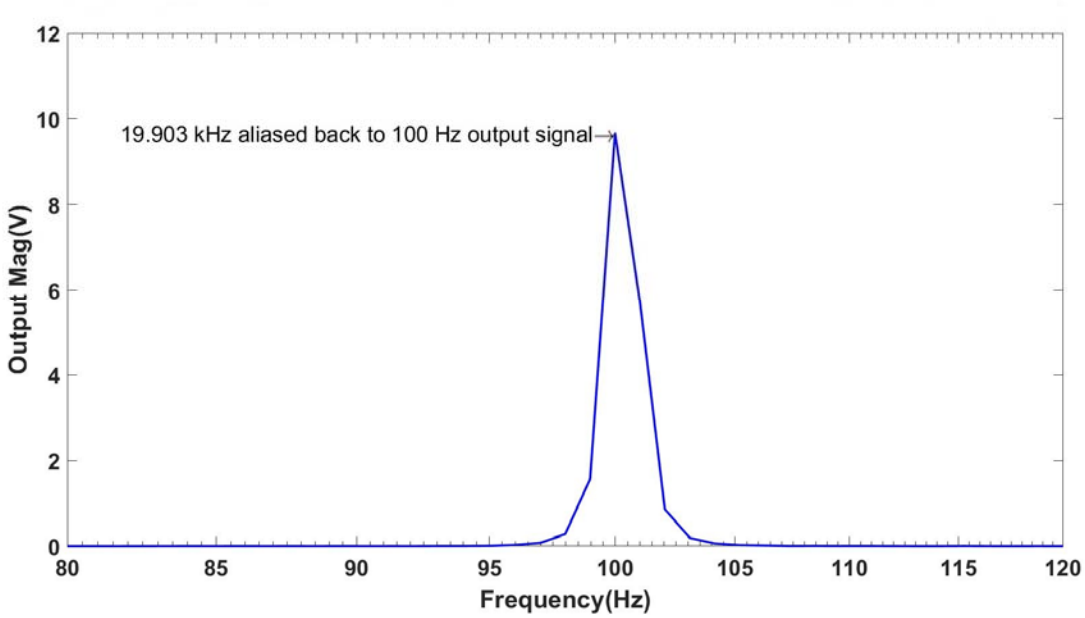
Please note that this 10 kHz is within the pass band of subsequent ADC anti-aliasing filter, and this clock feedthrough will manifest itself as a distortion to the testing signal.

The third drawback associated with programmable switched capacitor filter is aliasing. The programmable switched capacitor filter is essentially a sampled system, in which aliasing is an inherent problem. Frequency above one half the sampling frequency will be aliased back, and if the aliased signal falls within the passband of the filter, then it will be impossible to distinguish them from the real input signal. Figure 3.9 illustrates this phenomenon. In Figure 3.9, fixed 1V 20.103 kHz and 19.903 kHz signals are feed into the input of the filter respectively. If aliasing does not exit, those two signals will be easily eliminated according to Figure 3.7. Due to aliasing, those two signals are mixed down to 100 Hz by internal 20 kHz sampling frequency. This aliased output is a direct distortion to the real signal.



(a)

Figure 3.9 Aliasing for 21.103 kHz (a) signal



(b)

Figure 3.9(continued) and aliasing for 19.903 kHz (b) signal

In reality, even if those two signals does not exist in the system, aliasing still increases the output noise.

A simple way to reduce clock feedthrough and aliasing is to add an anti-aliasing filter before this programmable switched capacitor filter. However, this is not an applicable solution in this design because of the wide frequency range APS1006 covers. For 1 Hz center frequency, the filter clock frequency is 100 Hz and the internal sampling frequency is 200 Hz, which is also a frequency of interest in APCD measurement. The proposed anti-aliasing filter for 1 Hz will attenuate other useful frequencies. In short summary, multi-tone FFT is a nice idea but due to limitation from hardware implementation, this measurement scheme will not be adopted.

3.2.3 One Cycle Direct Calculation

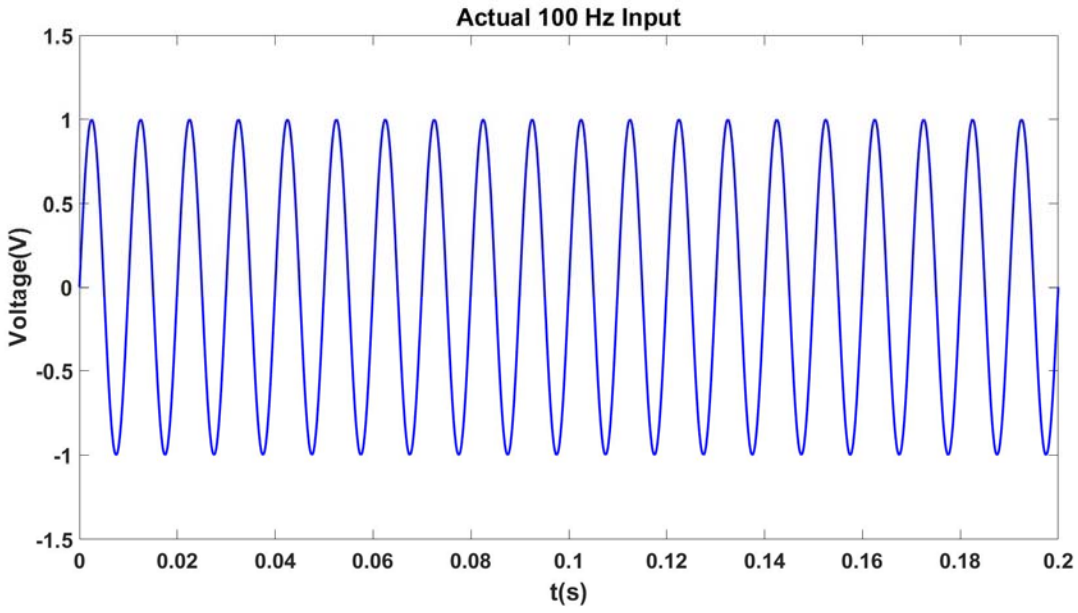
Revisit expression 3-1, we get

$$\text{output}[n] = \frac{1}{2^{\log 2(N)}} \sum_{k=0}^{N-1} \text{din}[n] \times e^{-j \times \frac{2\pi kn}{N}}$$

$$= \frac{1}{2^{\log 2(N)}} \sum_{k=0}^{N-1} \text{din}[n] \times [\text{Cos}(\frac{2\pi kn}{N})\text{-j Sin}(\frac{2\pi kn}{N})] \quad (3\text{-}2)$$

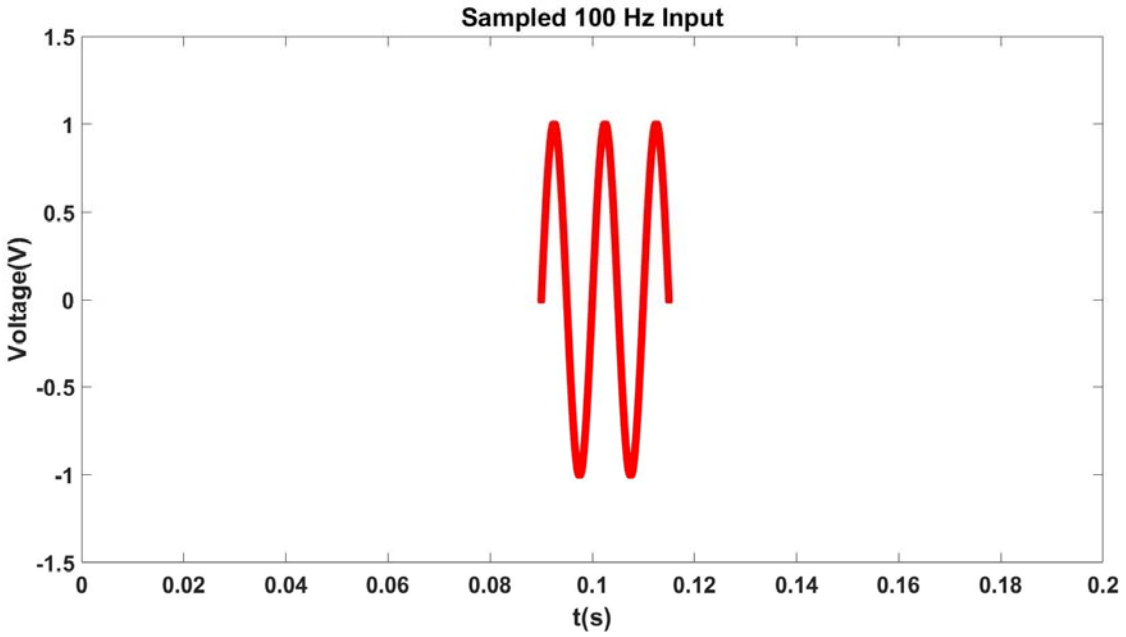
Expression 3-2 indicates that the real and imaginary part of complex phasor can be obtained by calculating the inner product of input array with $\text{Cos}(\frac{2\pi kn}{N})$ and - $\text{Sin}(\frac{2\pi kn}{N})$, respectively, if spectral leakage is ignored.

Generally speaking, spectral leakage occurs when the sampled input is not integral number of cycles. FFT assumes that the sampled data fully represents the actual input which is expected to repeat itself. Figure 3.10 illustrates the non-periodic sampling in time domain.

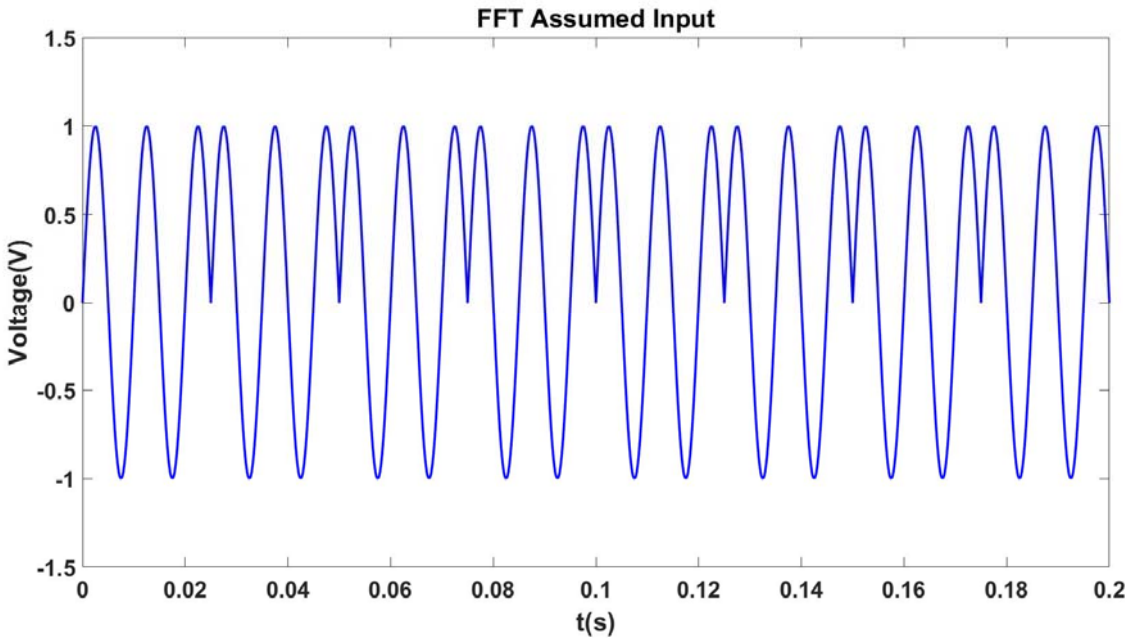


(a)

Figure 3.10 Actual 100 Hz input (a)



(b)



(c)

Figure 3.10(continued) sampled input(b) is not periodic and assumed input (c) is different from actual input (a)

As shown in Figure 3.10, the FFT assumed input is different from the actual input, which leads to spectral leakage in Figure 3.11.

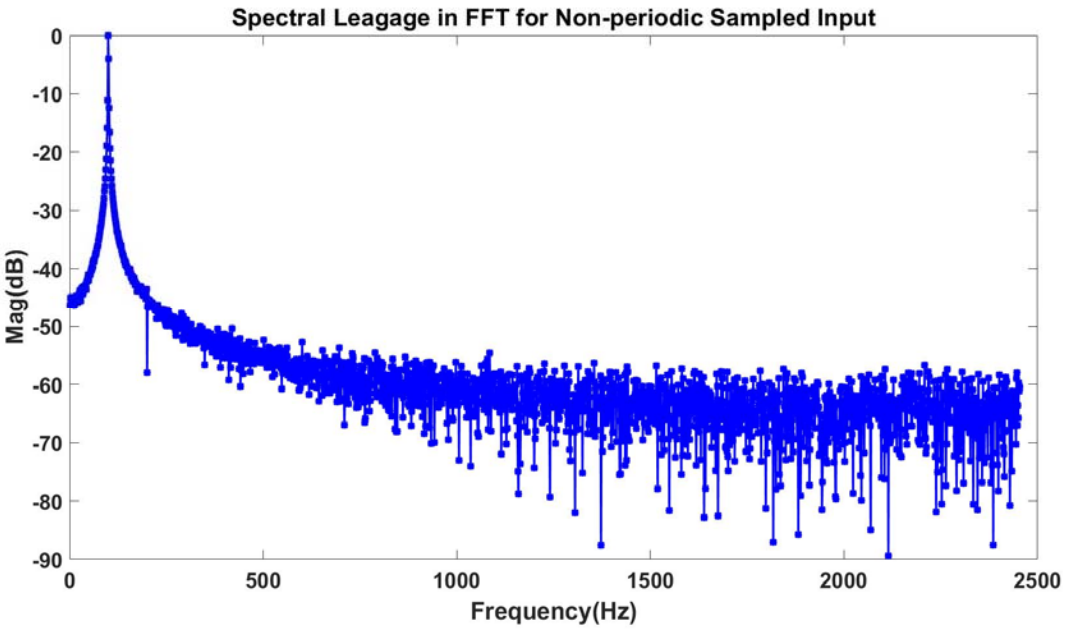


Figure 3.11 Spectral leakage in FFT

In order to combat spectral leakage, according to IEEE standard [38], coherent sampling should be used. The condition for coherent sampling is given by

$$\frac{f_{\text{in}}}{f_s} = \frac{M_{\text{cycle}}}{N_{\text{sample}}} \tag{3-3}$$

Where

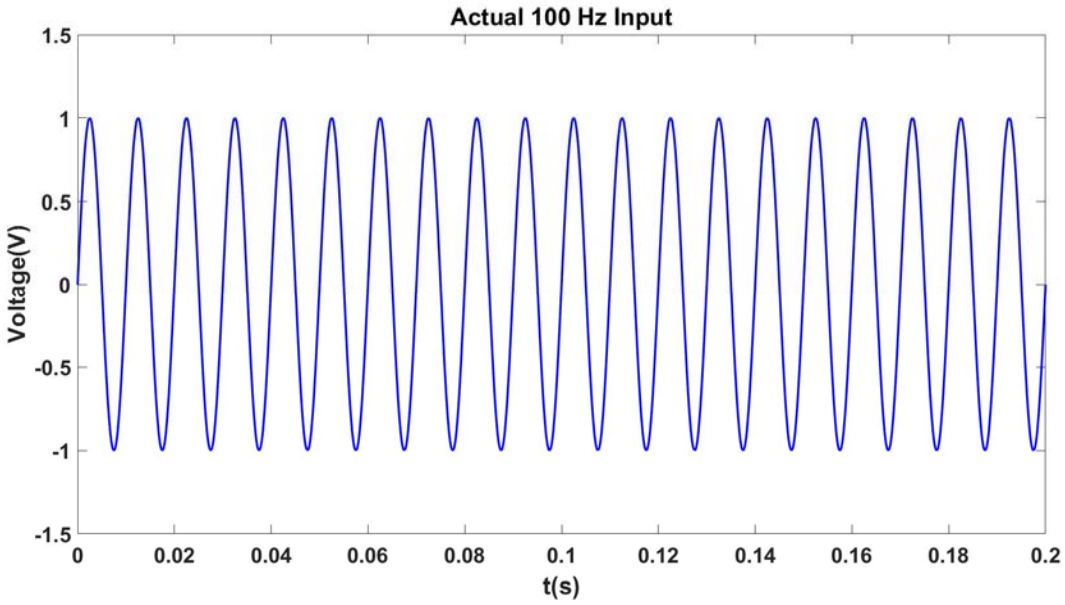
$$f_{\text{in}}: Input\ Signal\ Frequency$$

$$f_s: Sampling\ frequency$$

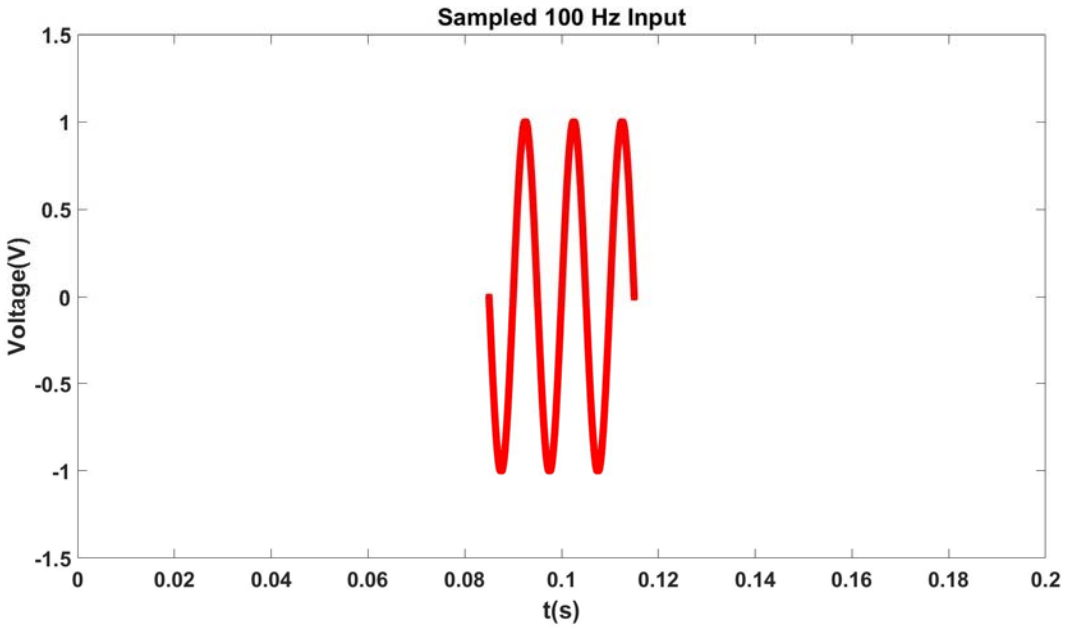
$$M_{\text{cycle}}: The\ number\ periods\ of\ input\ signal\ captured$$

$$N_{\text{sample}}: Must\ be\ a\ power\ of\ 2$$

For the best performance, M_{cycle} can be a prime number bigger than 2. Figure 3.12 illustrates coherent sampling in time domain.

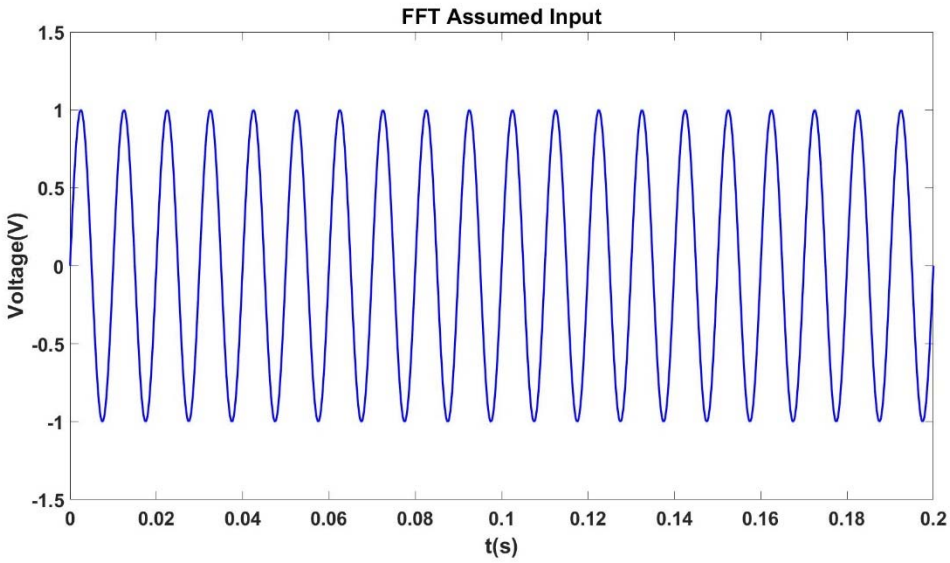


(a)



(b)

Figure 3.12 Actual input(a) and sampled input(b) for coherent sampling



(c)

Figure 3.12(continued) assumed input(c) for coherent sampling

Coherent dictates that there is an integer number of signal input captured in the sampled data array.

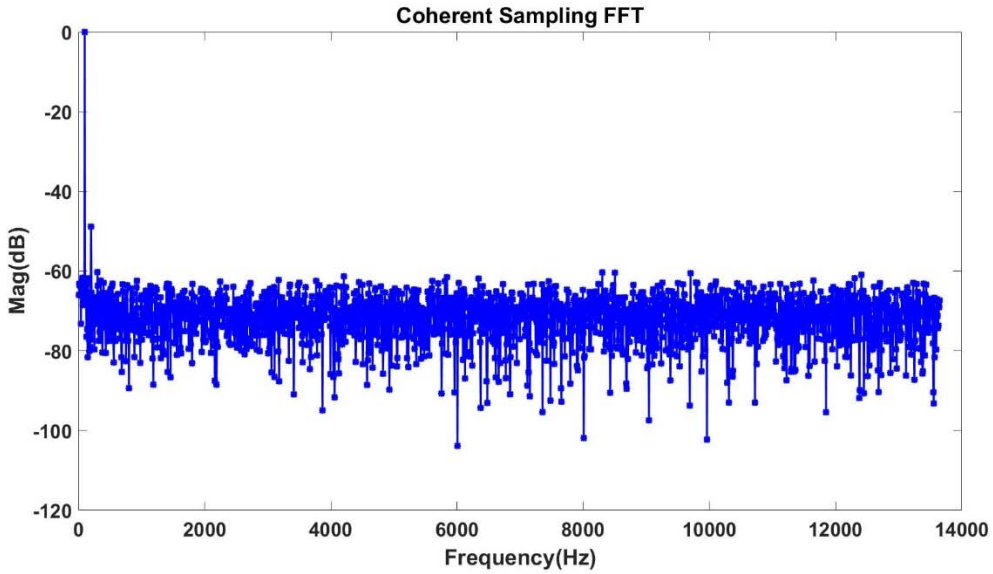


Figure 3.13 FFT result of coherent sampling. $f_{\text{in}} = 100\ Hz$, f_s=27307 Hz, M_{cycle}=15, N_{sample}=4096

If coherent sampling requirement is met, using expression 3-2, we can obtain the fundamental tone complex phasor directly, without calculating other bins in FFT spectrum.

Coherent sampling is widely used in analog to digital converter testing and evaluation. For ACPD application, this thesis proposes a very special case of coherent sampling that is not normally used in other areas. For 1 Hz to 100 Hz, as mentioned in section 3.2.1, the time for data acquisition is not acceptable if standard FFT procedure is used. But a special case of coherent sampling, where M_{cycle}=1, shall reduce the data acquisition time to minimum. The sampling clock and input signal are perfectly synchronized and controlled so that the sampling clock is 4096 times of input signal. In 4096 point data record, a complete cycle of input signal is captured, then the input signal's frequency domain information can be easily computed using expression 3-2.

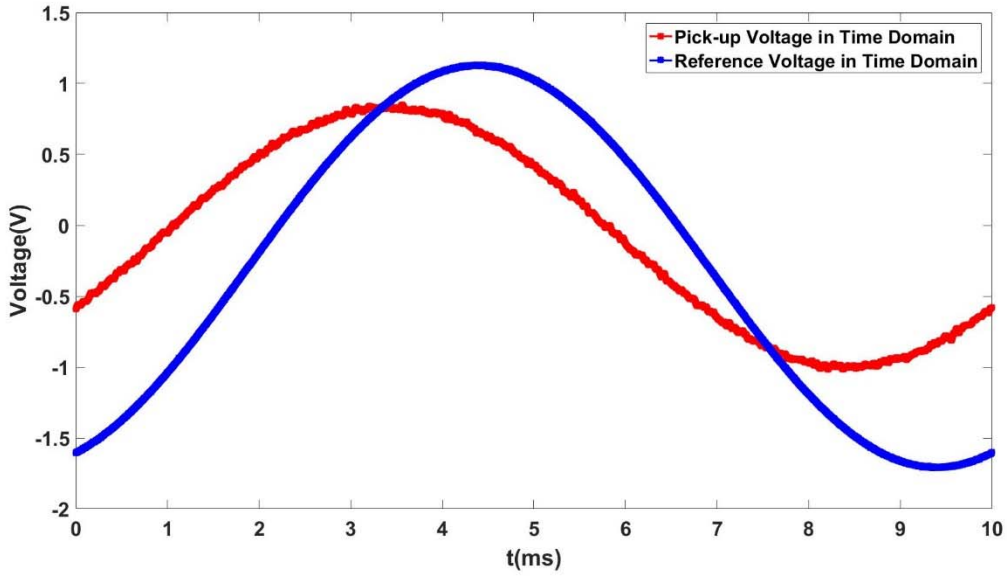


Figure 3.14 100 Hz pick-up and reference voltage sampled at 409.6 kHz for 4096 points

Please note that the pick-up voltage contains more noise than reference voltage, as expected. In hardware, the expression 3-2 can be implemented using Xilinx DSP48E1 slice [39].

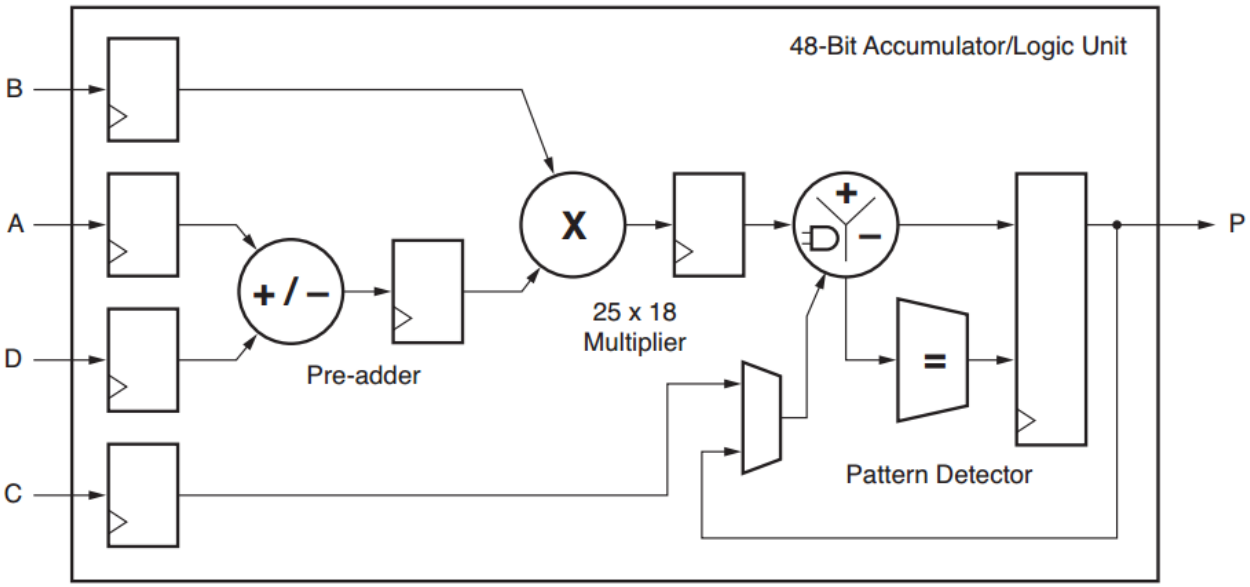


Figure 3.15[39] Basic DSP48E1 Slice Functionality

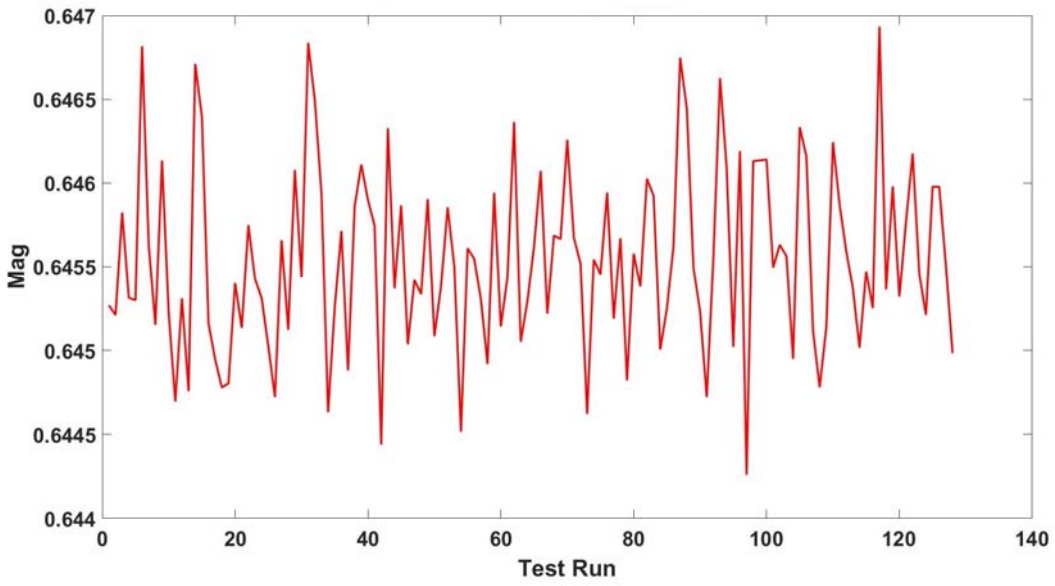
B is the sampled input from ADC, A is the base functions $\mathrm{Cos}(\frac{2\pi kn}{N})$ or -$\mathrm{Sin}(\frac{2\pi kn}{N})$, P is the multiply-accumulate output of A and B. The base functions are stored in a ROM memory in FPGA, which are essentially one cycle of Cos and Sin functions sampled by $\frac{2\pi}{4096}$ interval. The output P is the scaled version of right side of expression 3-2. Please note two individual DSP481E1 slices are used, one for real part calculation using $\mathrm{Cos}(\frac{2\pi kn}{N})$ as base function and the other for imaginary part calculation using -$\mathrm{Sin}(\frac{2\pi kn}{N})$ as base function. Implementing this procedure in FPGA is preferred because the calculation and data acquisition is completed simultaneously, liberating micro-controller from computationally intensive FFT calculation. Table 3.3 compares the results for 100 Hz ACPD measurement using FFT and one cycle direct calculation. The ratio between pick-up and reference is essentially the uncalibrated ACPD measurement data.

Table 3.3 Ratio between pick-up and reference

Method	Mag	Phase
Floating Point FFT	0.649131	26.367301 degree
One Cycle Direct Calculation	0.646139	34.808491 degree

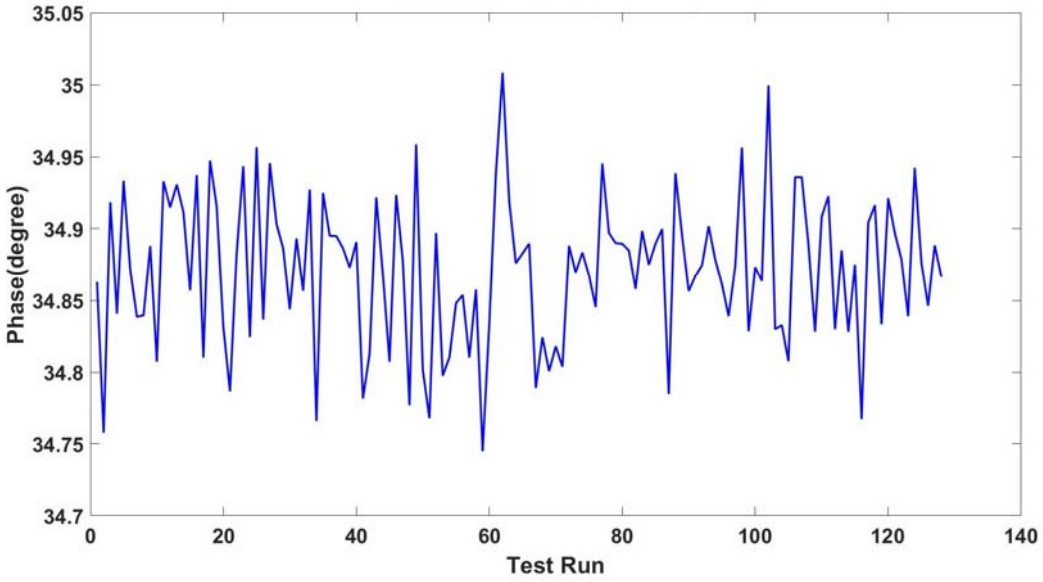
Even though the results from those two method are different, they are both valid from ACPD measurement point of view, because additional calibration process will eliminate this difference as long as the calibration process for a given frequency is done using the same method.

In order to evaluate the repeatability of this new procedure, the same one cycle direct calculation procedure is repeated by 128 times. Figure 3-16 shows the test results.



(a)

Figure 3-16 Repeatability test of one cycle direct calculation (a) magnitude result

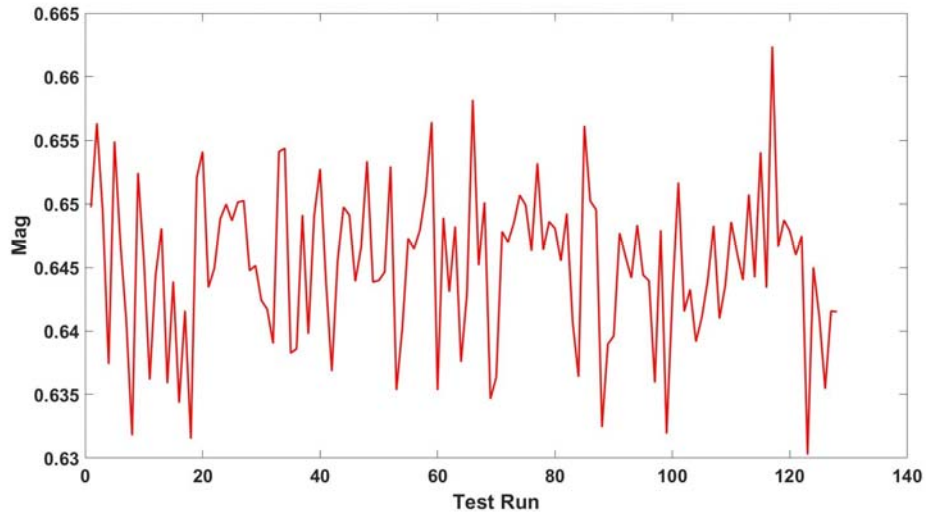


(b)

Figure 3-16(continued) and (b) phase result

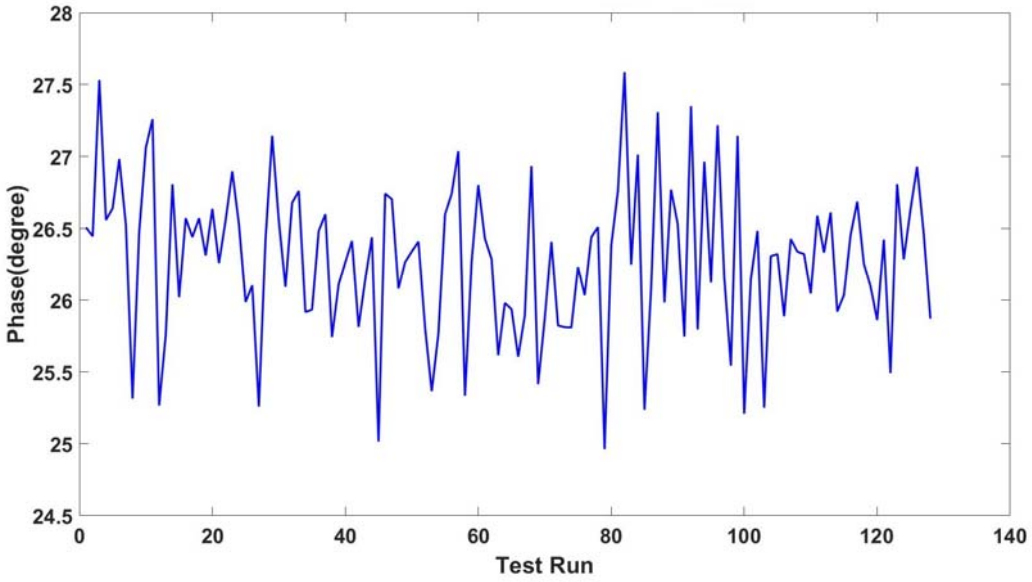
In Figure 3-16, the coefficient of variation for magnitude is 0.0845 % and the root-mean-square deviation for phase is 0.0517 degree.

The same repeatability test is performed using FFT method and Figure 3-17 is the result.



(a)

Figure 3-17 Repeatability test of FFT method (a) magnitude result



(b)

Figure 3-17(continued) and (b) phase result

In Figure 3-17, the coefficient of variation for magnitude is 0.948 % and the root-mean-square deviation for phase is 0.531 degree.

Table 3.4 Repeatability Test Comparison

Method	Coefficient of Variation for Mag	R.M.S Phase Error	Sampling Frequency	Data Acquisition Time
FFT	0.948 %	0.531 degree	4095 Hz	1000 ms
One Cycle Direct Calculation	0.0845 %	0.0517 degree	409.6 kHz	10 ms

As shown in Table 3.4, proposed method is much quicker and yet more accurate than classical FFT method.

3.2.4 Conclusion

In this section, single tone FFT, multi-tone FFT and one cycle direct calculation method are tested and compared. Table 3.5 lists the performance of those three approaches.

Table 3.5 Repeatability Test Comparison

Method	Speed	Accuracy	Hardware Cost	Comment
Single Tone FFT	Low	Medium	Medium	Requires high performance micro-controller
Multi-Tone FFT	Medium	Low	High	Not suitable for broadband ACPD measurement
One Cycle Direct Calculation	High	High	Low	Only applies to low frequency 1 Hz to 100 Hz. ADC sampling rate is limiting factor.

Using the last approach, the ADC sampling rate has to be significantly higher than the signal frequency, thus this approaches only applies to low frequency application. Fortunately, for ACPD measurement, low frequency data (1 Hz to 100 Hz) contains most of useful information.

3.3 System Calibration

3.3.1 Introduction and Basic Formulation

In Figure 2.2, the pick-up voltage and reference voltage are both amplified and filtered before feed into analog to digital converter for digitization. A chain of low noise amplifiers condition the weak raw pick-up voltage to a level that is comfortable for analog to digital converter. A bank of filters remove the noise in analog domain before digitization, so that the repeatability of the measurement can be guaranteed, as shown in Table 3.4. However, the uncalibrated ACPD measurement result, or the ratio between pick-up voltage and reference voltage is not very useful. Calibration data characterizes the transfer function of the amplifier and filter involved in previous

signal conditioning, and can be used to retrieve the actual ratio between pick-up voltage and reference voltage from uncalibrated version.

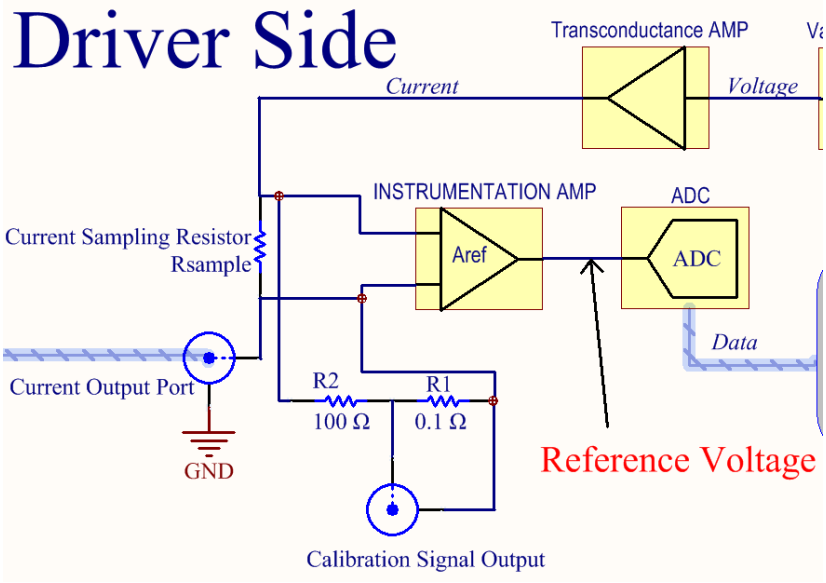


Figure 3.18 Calibration signal generation

Figure 3.18 illustrates the generation of calibration signal. The current sampling resistor R_{sample} converts the drive current is a differential voltage which is then attenuated by a resistor divider composed of R_1 and R_2 to a level that is similar to actual pick-up voltage. An instrumentation amplifier A_{ref} amplifies and converts this differential voltage to single end voltage for best analog to digital converter performance on the driver side. When calibration, the pick-up amplifier is connected to the calibration signal output instead of ACPD probe. Because the calibration output is a known signal from the driver's point of view, the ratio between pick-up voltage and reference voltage in this configuration is the calibration data.

In calibration configuration:

$$\frac{V_{\text{pk}}^{c}}{V_{\text{ref}}^{c}} = \frac{I^{c} \times R_{\text{sample}} \times \frac{R_1}{R_1+R_2} \times A_{\text{pk}}}{I^{c} \times R_{\text{sample}} \times A_{\text{ref}}} = \frac{R_1 \times A_{\text{pk}}}{(R_1+R_2) \times A_{\text{ref}}} \qquad (3\text{-}4)$$

V_{ref}^{c}: *reference voltage at ADC input in calibration configuration*

$$V_{\mathrm{pk}}^{c}: pick\ up\ \ voltage\ at\ ADC\ input\ in\ calibration\ configuration$$

$$I^{c}: drive\ current\ in\ calibration\ configuration$$

$$A_{\mathrm{ref}}: driver\ side\ amplifier\ transfer\ function$$

$$A_{\mathrm{pk}}: pick\ up\ side\ amplifier\ and\ filter\ transfer\ function$$

In measurement configuration:

$$\frac{V_{\mathrm{pk}}}{V_{\mathrm{ref}}} = \frac{\Delta \mathrm{V} \times A_{\mathrm{pk}}}{I \times R_{\mathrm{sample}} \times A_{\mathrm{ref}}} \tag{3-5}$$

$$V_{\mathrm{ref}}: reference\ voltage\ at\ ADC\ input\ in\ measurement\ configuration$$

$$V_{\mathrm{pk}}: pick\ up\ \ voltage\ at\ ADC\ input\ in\ measurement\ configuration$$

$$I: drive\ current\ in\ measurement\ configuration$$

$$\Delta V: actual\ pick\ up\ voltage\ between\ probe\ pins$$

From 3-4 and 3-5, the normalized potential drop can then be expressed as:

$$\frac{\Delta \mathrm{V}}{I} = \frac{V_{\mathrm{pk}}}{V_{\mathrm{ref}}} \times \frac{R_{\mathrm{sample}} \times A_{\mathrm{ref}}}{A_{\mathrm{pk}}} = \frac{V_{\mathrm{pk}}}{V_{\mathrm{ref}}} \times \left(R_{\mathrm{sample}} \times \frac{R_1 \times V_{\mathrm{ref}}^{c}}{(R_1 + R_2) \times V_{\mathrm{pk}}^{c}}\right) \tag{3-6}$$

The item in the parentheses on the right side of 3-6 is the calibration data, which derives from calibration mode result, current sample resistor and resistor divider. Using 3-6, raw measurement data $\frac{V_{\mathrm{pk}}}{V_{\mathrm{ref}}}$ can be converted to normalized potential drop $\frac{\Delta \mathrm{V}}{I}$ with the help of calibration data that has been obtained in prior calibration procedure.

3.3.2 Resistor Selection for Accurate Calibration

As shown in expression 3-6, the accuracy of current sampling resistor and resistor divider determine the quality and reliability of calibration. For different frequency range, the design strategy is different. For low frequency range, or 1 Hz up to 1 kHz, thermal stability is major concern, while for 1 kHz and above, parasitic series inductance introduces most of the error.

As shown in figure 2.33, the maximum output current for low frequency range can be as high as 3.5 amps in amplitude. The current sampling resistor temperature rise due to self-heating must be kept minimum.

Resistors using different technologies do not perform significantly different at a first glance. However, the resistors' electrical performance, stability and behaviors after installation are heavily influenced by its resistance material, implementation and processing. Important parameters to consider when selecting approximate resistors are sensitivity to electrostatic discharge (ESD), temperature coefficient (TCR), Tolerance, Thermal Stabilization, noise and long-term stability [40]. The most common resistor technologies are wirewound, thin film, thick film and bulk metal foil [40].

The precision wirewound resistor is manufactured by winding resistance wire around a ceramic or plastic bobbin. The resistance value is controlled by varying the wire diameters, lengths as well as alloy type. Precision wirewound resistors are less sensitive to ESD than thin film and thick film resistors. It also has less noise, lower TCR and higher long term stability than thin film and thick film resistor.

Figure 3.19 Construction of wirewound resistors. [41]

As shown in Figure 3.19, wirewound resistors have a coiled wire structure, which leads to significantly amount of parasitic inductance and capacitance. Thus wirewound resistors are not suitable for high speed applications.

Thin film resistors consist of an extremely thin layer of resistive material deposited on a ceramic or silicon substrate [40]. Thin films can yield a higher resistance per area than wirewound resistors. However, due to its construction, the stability, TCR and ESD capability of thin film resistors are not as good as some other types of resistors. Thin film resistors are suitable for application requires intermediate level of precision.

Another type of common resistors are thick film resistors which are comprised of ceramic based materials combined with metallic particles [40]. The advantage of this kind of resistors is low cost. In terms of other critical properties, thick film resistors performs poorly.

Bulk metal foil resistors are based on a special concept where a bulk metal cold-rolled foil is cemented to a ceramic substrate. It is then photoetched into a resistive pattern. Later, it is laser adjusted to any desired value and tolerance [40]. Bulk metal foil resistors are not commonly used, partially due to its high price. However, bulk metal foil resistors have a number of characteristics that make them superior to both thin film and thick film resistors.

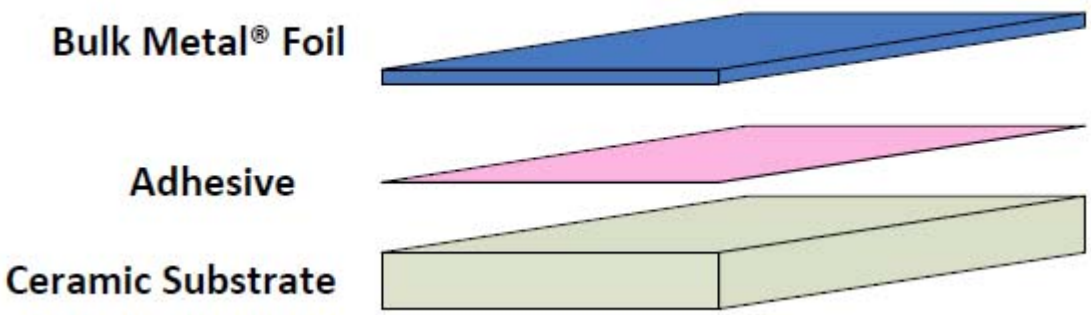


Figure 3.20 Structure of bulk metal foil resistors. [40]

Bulk metal foil resistors achieve maximum stability and near-zero TCR [40], as shown in Figure 3.21.

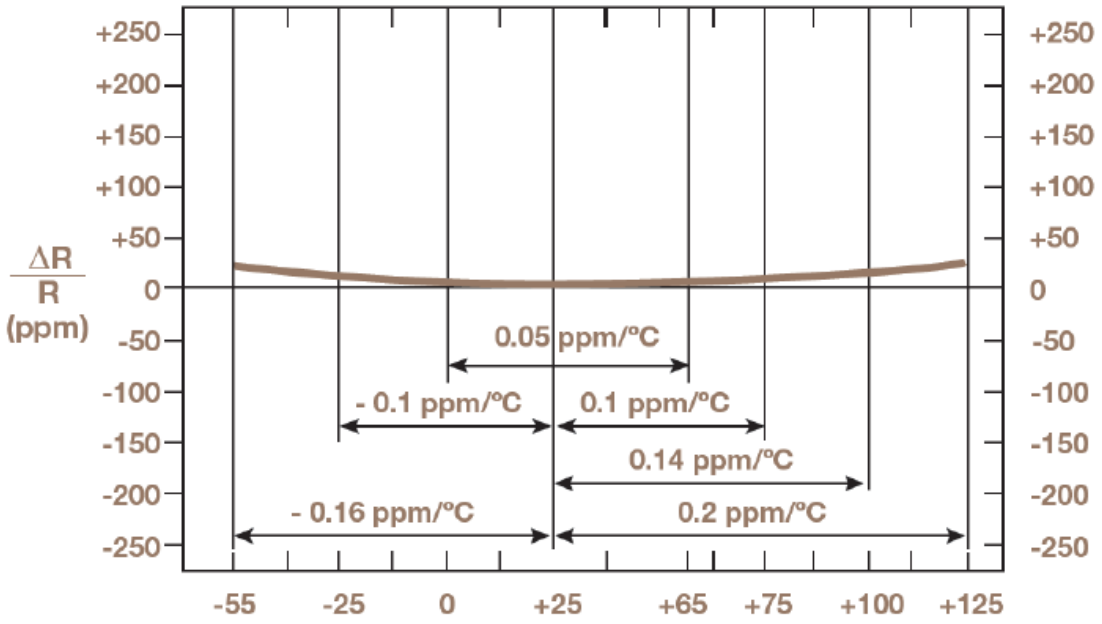


Figure 3.21 Ambient temperature coefficient and TCR performance of bulk metal foil resistors. [40]

Technology	Temperature Coefficient of Resistance (TCR) -55°C to +125°C, +25°C Ref.	Initial Tolerance	End of Life Tolerance	Load Life Stability at +70°C, Rated Power 2000 Hours and 10,000 Hours	ESD (V)	Thermal Stabilization	Noise (dB)
Bulk Metal Foil	0.2 ppm/C	From 0.005%	< 0.05%	0.005% (50 ppm) 0.01% (100 ppm)	25,000	<1 Second	-42
High Precision Thin Film	5 ppm/C	From 0.05%	< 0.4%	0.05% (500 ppm) 0.15% (1500 ppm)	2500	> few minutes	-20
Precision Thick Film	50 ppm/C	From 0.5%	< 5%	0.5% (5000 ppm) 2% (20,000 ppm)	2000	> few minutes	+20
Wirewound	3 ppm/C	From 0.005%	< 0.5%	0.05% (500 ppm) 0.15% (1500 ppm)	5000	> few minutes	-35

Figure 3.22 Characteristics of different types of resistors [42]

Figure 3.22 summaries the characteristics of different types of resistors. For ACPD calibration circuit, at low frequency (<1 kHz), the current sampling resistor must be bulk metal foil resistor and the resistor divider can either be high precision thin film resistor or bulk metal foil resistor.

For higher frequency, large drive current is not necessary and thus the emphasis should be focused on reducing error due to parasitic inductance. As a first order approximation, the parasitic effects of an actual resistor can be modeled using lumped circuit in Figure 3.23.

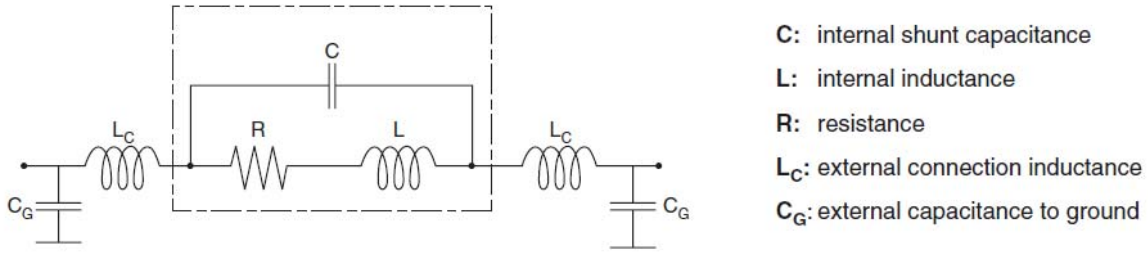


Figure 3.23 Typical high frequency resistor lumped circuit model [43]

For typical ACPD application where frequency is lower than 100 kHz, the internal inductance L affect the overall accuracy most significantly. According to the datasheet of typical bulk metal foil resistor [44], the internal inductance is approximately 5 nH, which gives rise to 3 % error for a 100 mΩ current sampling resistor at 100 kHz. Apparently, at such high frequency, bulk metal foil resistor is not the best choice. In this scenario, high frequency precision thin film resistor is the best candidate [45]. Figure 2.24 gives the parasitic inductance and capacitance for MCT 0603 and MCT 0603 HF series

Flat Chip Resistors MCT 0603 and MCT 0603 HF (valid thru 10 GHz)

	MCT 0603		MCT 0603 HF	
R / Ω	*L* / nH	*C* / pF	*L* / nH	*C* / pF
5,6	0,75	0,035	0,60	0,03
10	0,85	0,035		
15	0,78	0,035	0,55	0,03
39	0,80	0,035	0,55	0,03
50	**0,85**	**0,035**	**0,67**	**0,03**

Figure 3.24 Parasitic inductance and capacitance for MCT 0603 and MCT 0603 HF series [45]

Similarly, for MCT 0603 series, the internal inductance only introduces 0.047% error for a 1 Ω current sampling resistor at 100 kHz.

In some special cases, ACPD measurement can be done at 1 MHz to 10 MHz range. In this frequency range, special procedure must be adopted to minimize the side effect of parasitic inductance. The first and more direct approach is to use very low parasitic inductance high frequency resistor, such as Vishay FC series [46].

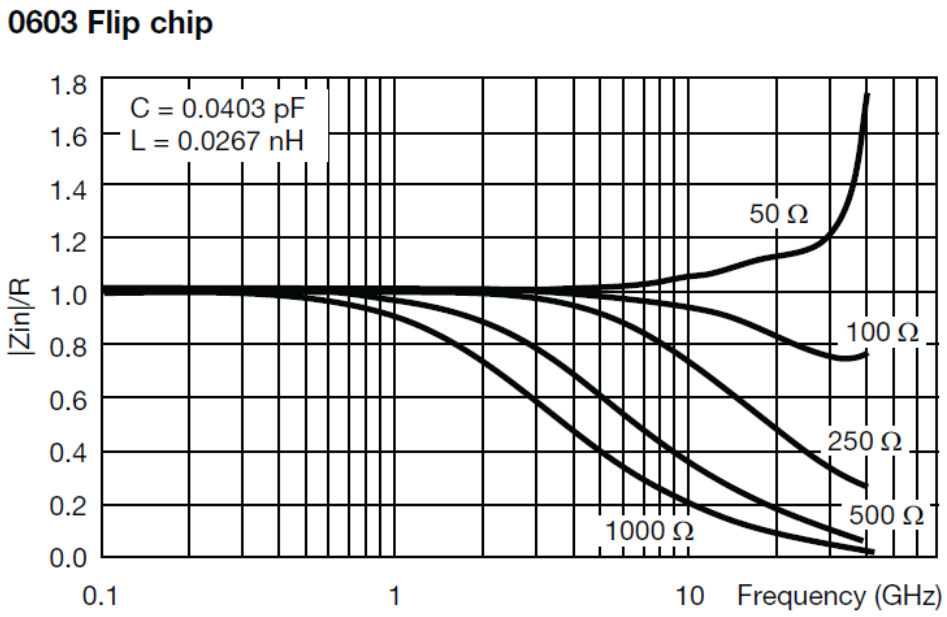


Figure 3.24 FC series 0603 flip chip package impedance [46]

FC series high frequency resistor has extremely low parasitic inductance (0.0267 nH), which introduces negligible error even at 10 MHz.

The second and more complicated approach is to accurately measure this parasitic inductance L and include it in the calibration data. Detailed discussion on this topic is out of the scope of this thesis and can be found in reference [47]. As shown in Figure 2.25, the basic idea is that Port 1 is used to drive current through the DUT and port 2 is used to measure the voltage generated across the DUT.

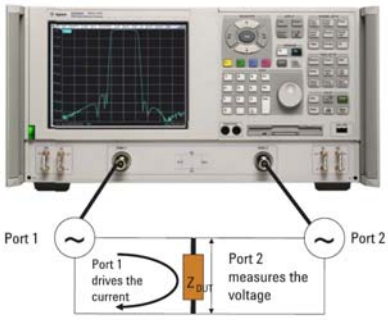


Figure 3.25 Two port measurement for ultra-low impedance DUT

For a 50Ω system, the impedance of DUT can be expressed as [47]

$$Z_{\mathrm{DUT}} = 25 \times \frac{S_{21}}{1-S_{21}} \Omega \tag{3-7}$$

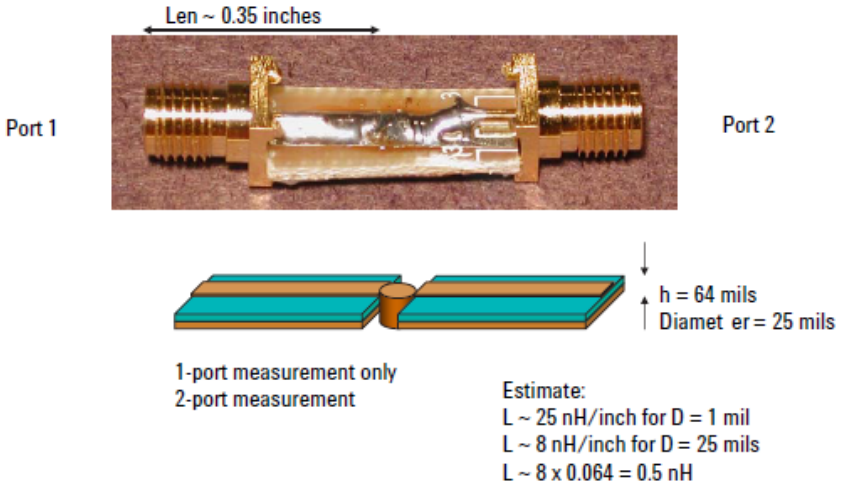


Figure 3.26 Two-port shorted via measurement setup [47]

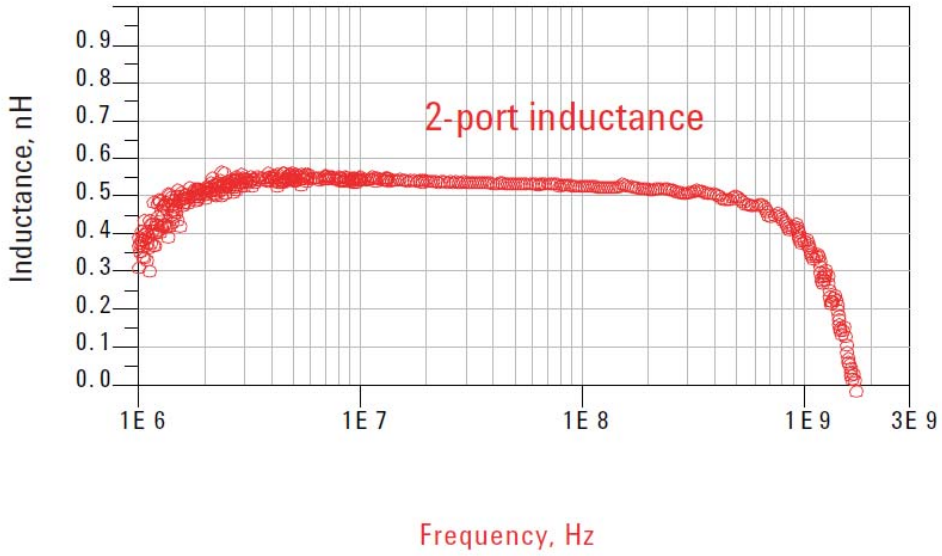


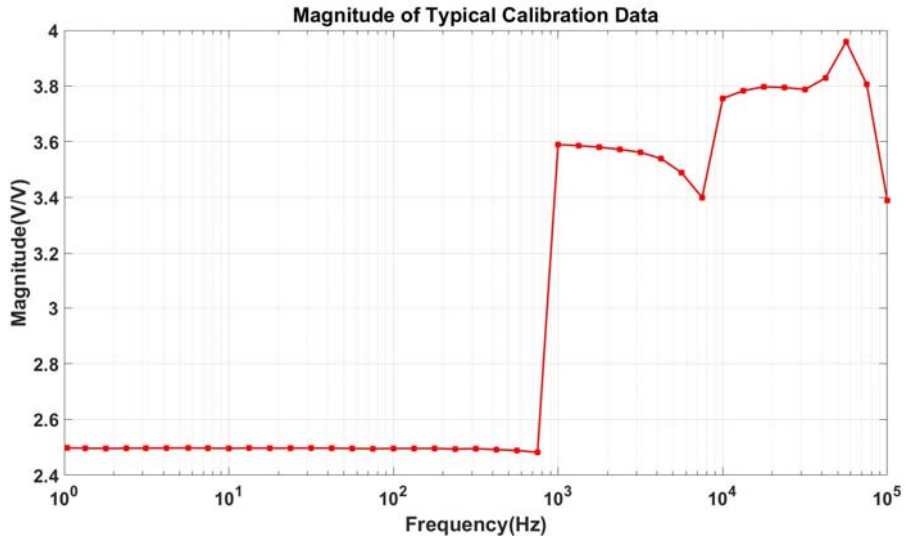
Figure 3.27 Two-port shorted via measurement result [47]

As shown in Figure 3.26 and 3.27, the inductance of a typical via can be measured using this method. Please note that the measured 0.54 nH value, is very close to the estimated value of 0.5 nH, assuming the via is a 64 mil long and 25 mil diameter rod.

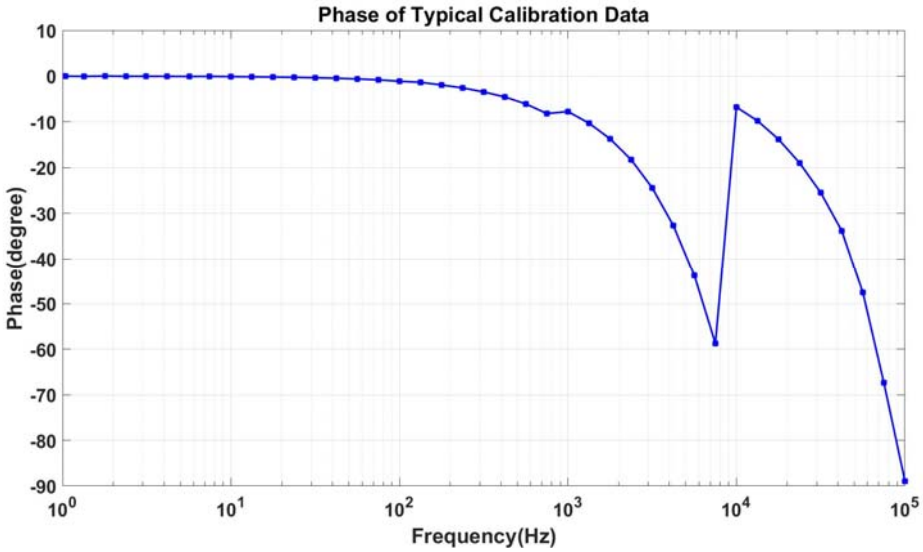
Table 3.6 Resistor Selection of Accurate Calibration

Frequency Range	Current Sampling Resistor	Resistor Divider
DC- 1 kHz	Bulk metal foil resistor	Precision thin film resistor
1 kHz-100 kHz	Precision thin film resistor	Precision thin film resistor
100 kHz-10 MHz	High frequency precision thin film resistor	High frequency precision thin film resistor

3.3.3 Typical Calibration Data



(a)



(b)

Figure 3.28 Typical calibration data

Please note that in Figure 3.28, two factors contribute to the discontinuity of the calibration data: transconductance amplifier change and pick-up signal filter change. At 1 kHz, system starts to use

high frequency transconductance amplifier instead of high current transconductance amplifier; at 10 kHz, system switches from LP_2 to LP_3 in Table 2.3.

3.4 Conclusion

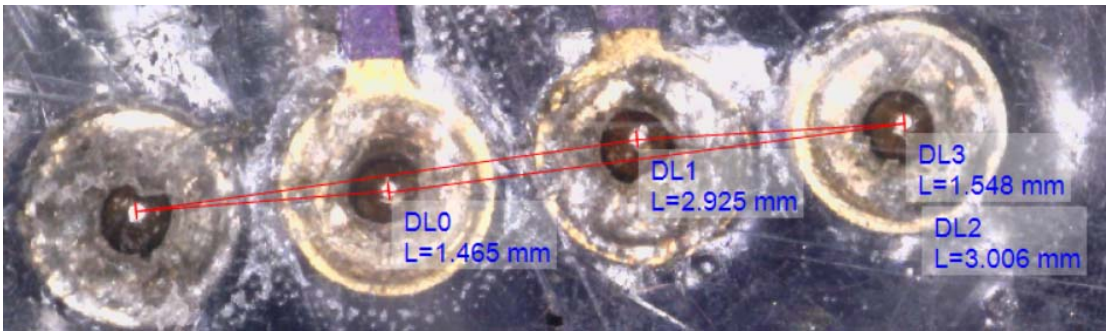
This chapter mainly discusses low level signal processing and calibration. The main task of the signal process is to convert captured time domain waveform into frequency domain complex phasor. Conventional Fast Fourier Transform proves to be a viable method but its data acquisition time is unacceptably long for an ultra-fast ACPD measurement system. A special case of coherent sampling, where the cycle of sampled signal equals to one, is exploited. This new approach provides very high precision and minimum time penalty.

A general purpose calibration method for ACPD is introduced in this chapter. The accuracy of this calibration method relies on strategically chosen resistor type. Different types of resistors are suitable for different scenarios which is summarized in Table 3.5. In next chapter, verification and test of this new instrument will be discussed.

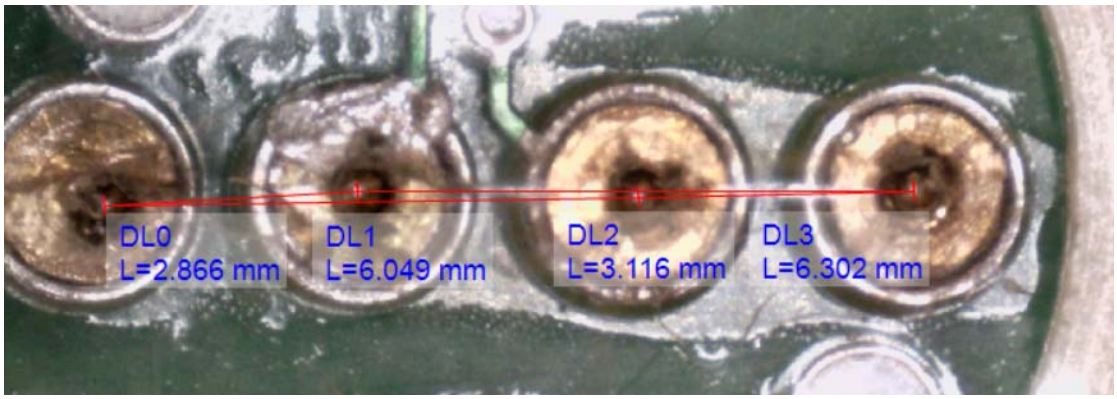
CHAPTER 4. TEST AND VERIFICATION

4.1 ACPD Probe Pin Separation Measurement

Before conducting ACPD measurement, the probe pin separation must be accurately measured, since it has significant impact on the interpretation of ACPD data. A digital USB microscope is used for this purpose. All measurements shown in Figure 4.1 are after microscope calibration.

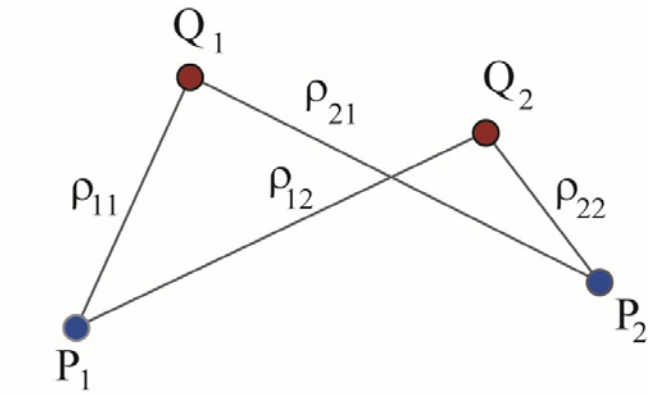


(a)



(b)

Figure 4.1 ACPD probe pin separation measurement for (a) 1.5 mm probe and (b) 3.0mm probe



(c)

Figure 4.1(continued) with pin arrangement illustrated in (c)

Table 4.1 summaries measured pin separation for 1.5 mm pin separation and 3 mm pin separation probe .

Table 4.1 Measured pin separation

	3.0 mm probe	**1.5 mm probe**
ρ_{11}	2.866 mm	1.465 mm
ρ_{12}	6.049 mm	2.925 mm
ρ_{22}	3.116 mm	1.548 mm
ρ_{21}	6.302 mm	3.006 mm

4.2 System Speed Test

Ultra high measurement speed is one of the many advantages of this new ACPD system as shown in the test below. Table 4.2 lists the measurement configuration of a typical wide band ACPD experiment. Figure 4.2 shows the measurement log output from the ACPD software.

Table 4.2 Speed test parameters

Parameter	Value
Start frequency	1 Hz
Stop frequency	100 kHz
Number of points per decade	8
Total number of points	41
Frequency spacing	logarithmically

```
Freq: 1778.304577 Hz Mag 0.412389 Phase: -149.110430 degree
Freq: 2371.370792 Hz Mag 0.475073 Phase: -153.816876 degree
Freq: 3162.324429 Hz Mag 0.546174 Phase: -160.105192 degree
Freq: 4217.028618 Hz Mag 0.625013 Phase: -168.526510 degree
Freq: 5623.400211 Hz Mag 0.709252 Phase: -179.795119 degree
Freq: 7499.009371 Hz Mag 0.791895 Phase: 165.162081 degree
Freq: 10000.020266 Hz Mag 0.995243 Phase: -142.419601 degree
Freq: 13335.198164 Hz Mag 1.153507 Phase: -145.188128 degree
Freq: 17782.747746 Hz Mag 1.336188 Phase: -148.938848 degree
Freq: 23713.707924 Hz Mag 1.545569 Phase: -154.011174 degree
Freq: 31622.797251 Hz Mag 1.782502 Phase: -160.839547 degree
Freq: 42169.690132 Hz Mag 2.042222 Phase: -169.927389 degree
Freq: 56234.151125 Hz Mag 2.308284 Phase: 177.795734 degree
Freq: 74989.348650 Hz Mag 2.566848 Phase: 162.131195 degree
Freq: 100000.053644 Hz Mag 2.735208 Phase: 140.603139 degree
CURRENT OUT SHORT TO GND

Elapsed time is 14.512033 seconds.
```

Figure 4.2 Measurement speed test session output log (partial)

As shown in Figure 4.2, the frequency scan using parameter in Table 4.2 takes 14.5 seconds to complete, which is significantly faster than any other ACPD systems ever built. Similar experiment would cost more than 12 hours to complete if distributed ACPD system were used.

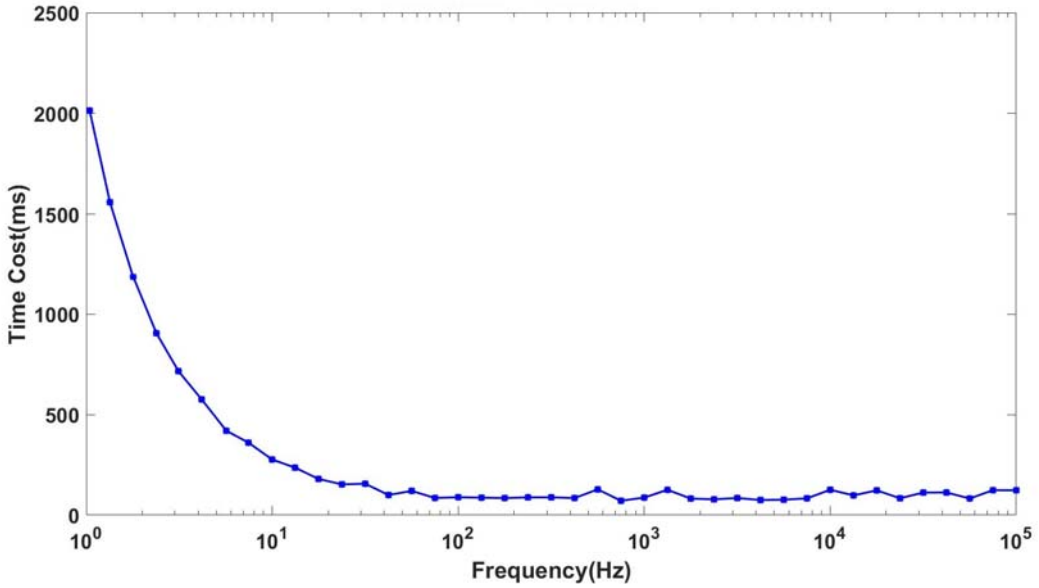


Figure 4.3 Time cost for each frequency

As shown in Figure 4.3, time cost decreases as frequency increases for low frequency, but after 100 Hz, the time cost per point levels off. This is because before 100 Hz, data acquisition time dominates the overall time cost, while signal processing is only a small portion of total time cost. As frequency increases, data acquisition time decreases proportionally, while signal processing time stays constant.

Table 4.2 Time Cost per Decade

Frequency /Hz	Time /second	Percentage /%
[1,10)	7.74	67.6
[10,100)	1.31	11.4
[100,1000)	0.72	6.3
[1000,10000)	0.69	6.1
[10000,1000000]	0.99	8.6

As expected, the majority of time is spent on the first decade, which means that if the scan starts at 10 Hz, the total time cost can be reduced to 4.7 seconds. For real world application, this time can be further shortened by reducing the number of points per decade frequency.

4.3 System Repeatability Test

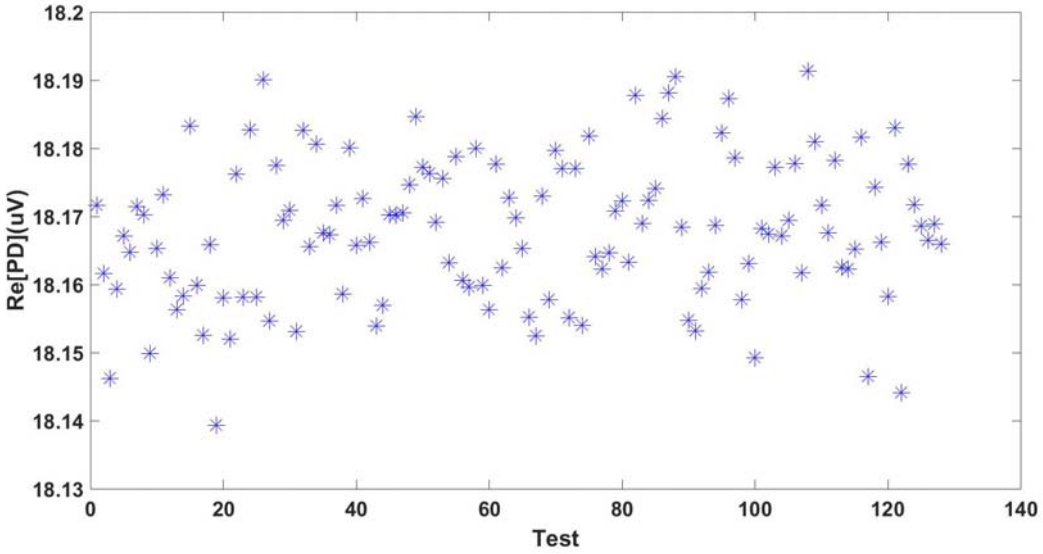
In order to evaluate the precision of this system, ACPD measurement at 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz are repeated 128 times. From the coefficient of variation for the real part of potential drop, the system repeatability performance can be assessed.

Table 4.4 System repeatability at typical frequencies

Frequency /Hz	Coefficient of Variation /%	SNR /dB
10	0.058	64.7
100	0.036	68.9
1000	0.039	68.2
10,000	0.030	70.5
100,000	0.629	44.0

For frequency equal or lower than 10 kHz, the system is very repeatable, indicating a very low overall system noise. However, for frequency close to 100 kHz, the noise increases dramatically. For most ACPD applications, 1 Hz to 10 kHz is of the most interest, but future effort must be allocated to improve the noise performance of the system at higher frequencies. Please note that this section only takes the noise from electronic system into consideration. In reality, other factors, including probe pin location uncertainly as well as material inhomogeneity also contribute to the uncertainty of ACPD measurement. In order to minimize probe associated measurement error, the

pin location must be well defined from a mechanical design point of view. Figure 4.4 to Figure 4.8 demonstrate the measurement error at each typical frequencies.



(a)

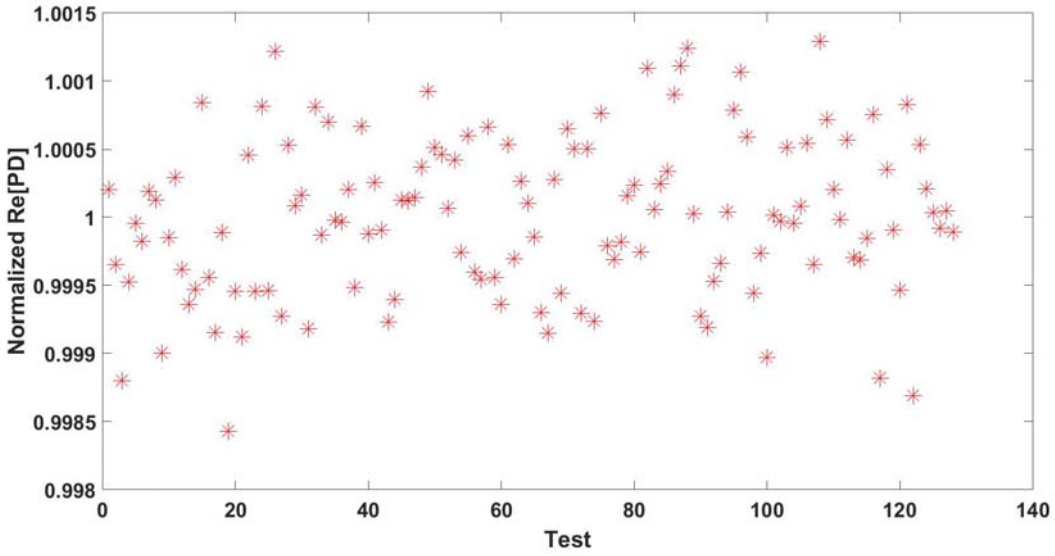
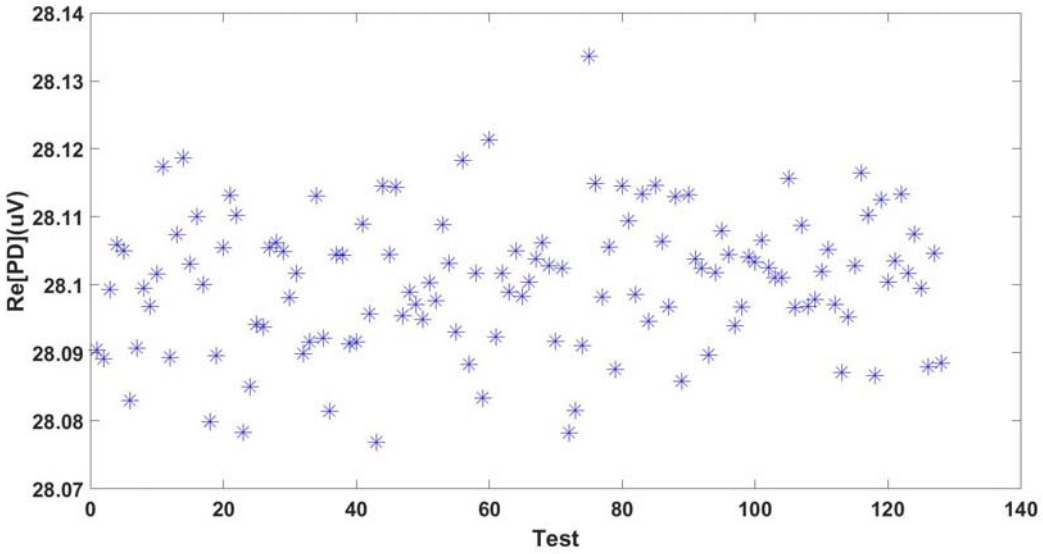
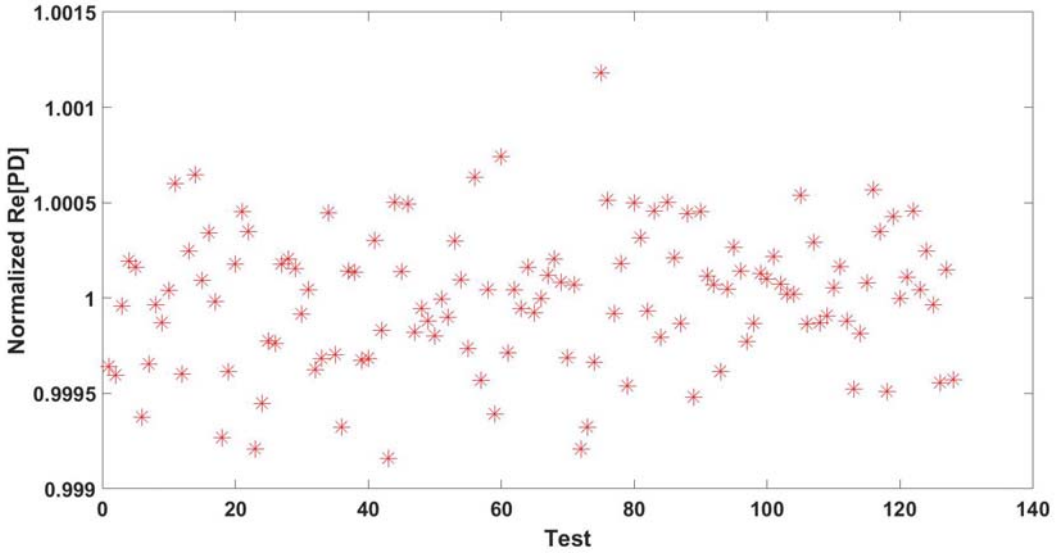


Figure 4.4 System repeatability test at 10 Hz: (a) real part of potential drop (b) real part of potential drop normalized by average value

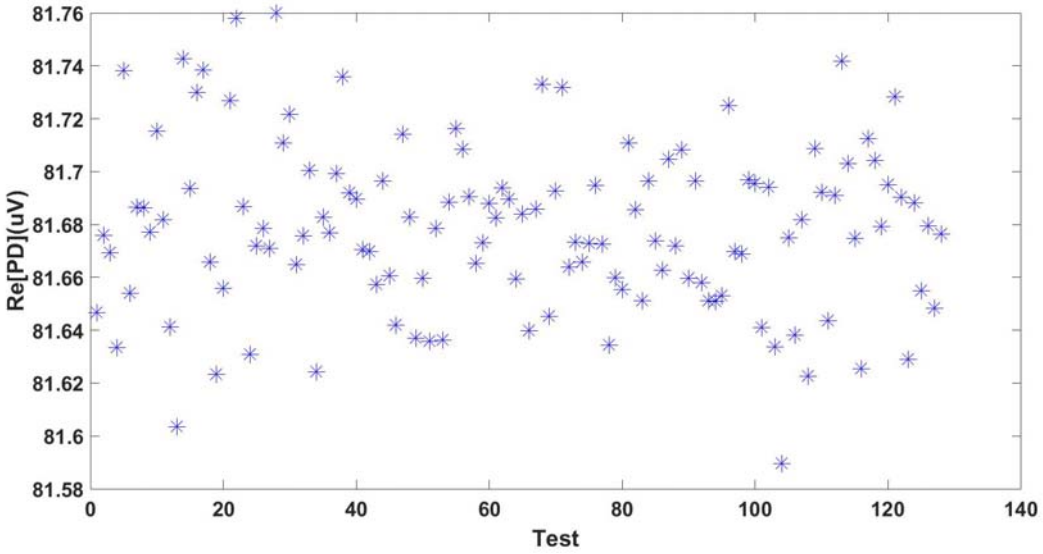


(a)

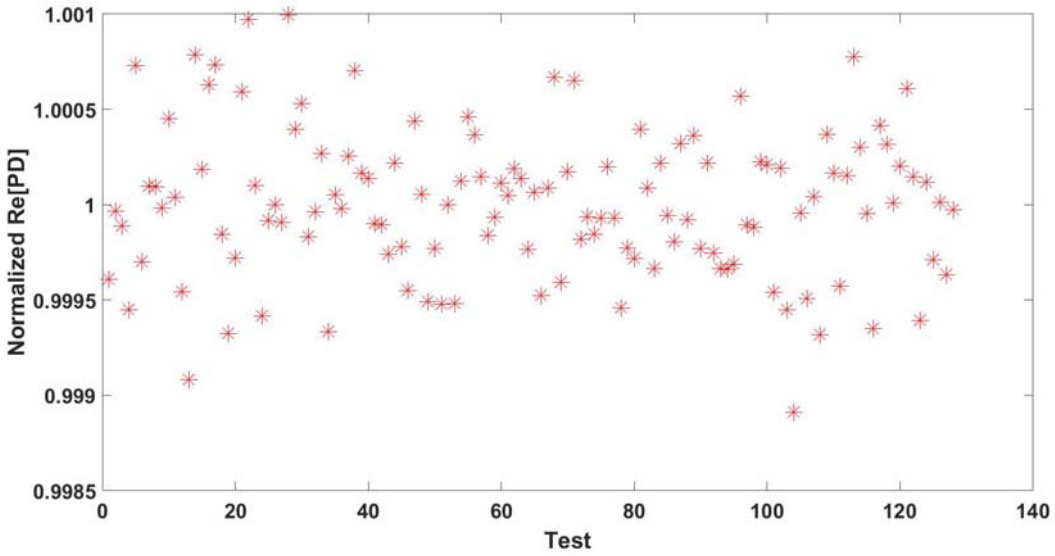


(b)

Figure 4.5 System repeatability test at 100 Hz: (a) real part of potential drop (b) real part of potential drop normalized by average value

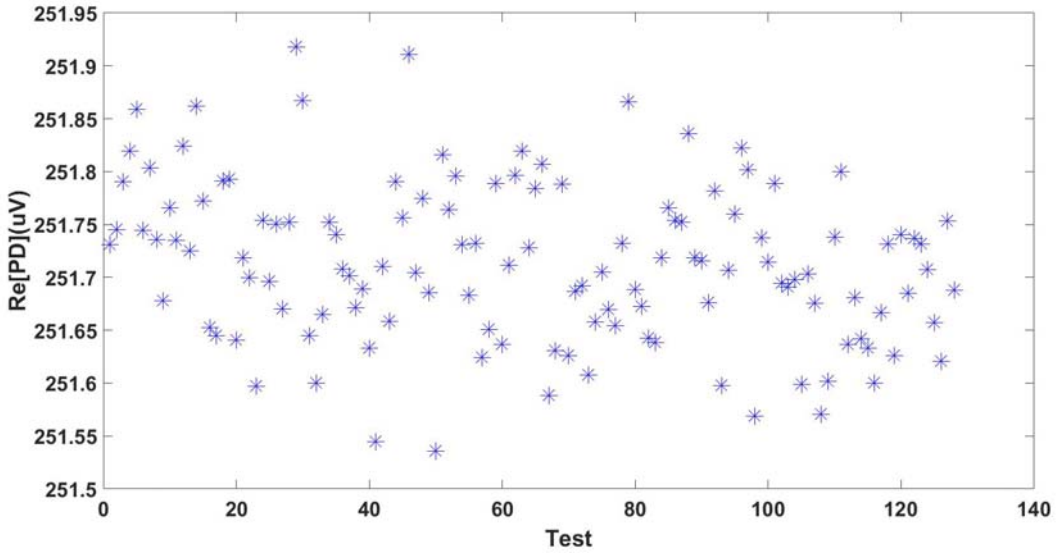


(a)

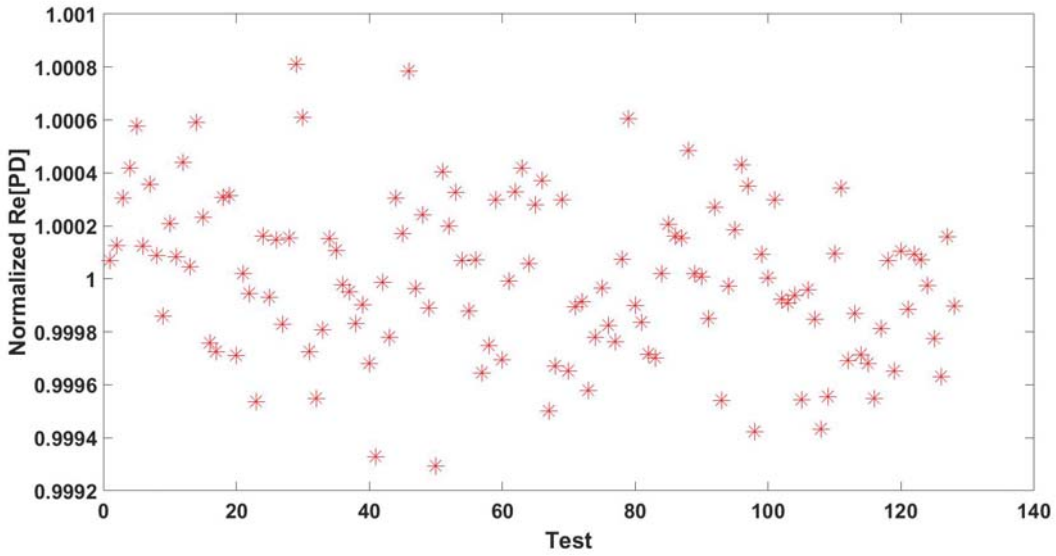


(b)

Figure 4.6 System repeatability test at 1 kHz: (a) real part of potential drop (b) real part of potential drop normalized by average value

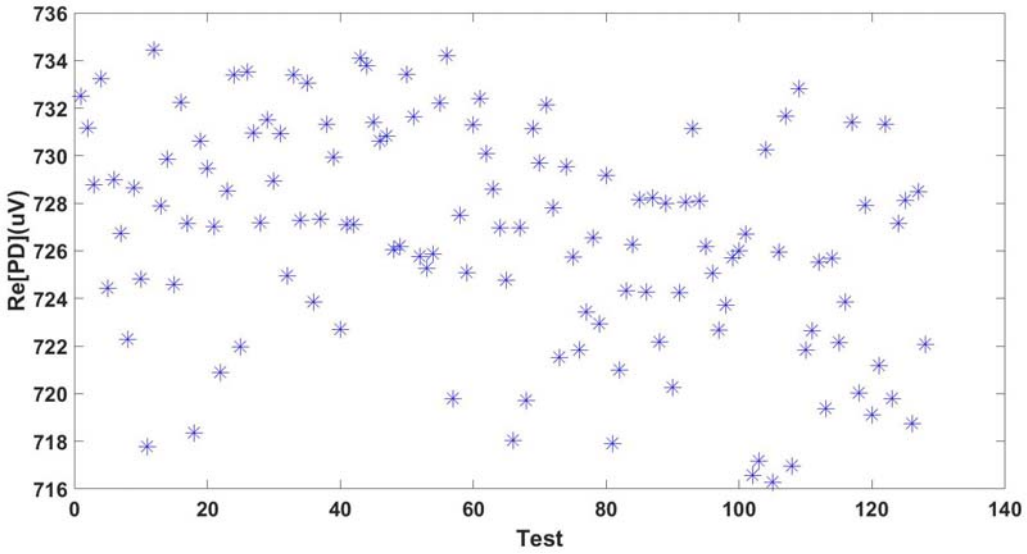


(a)

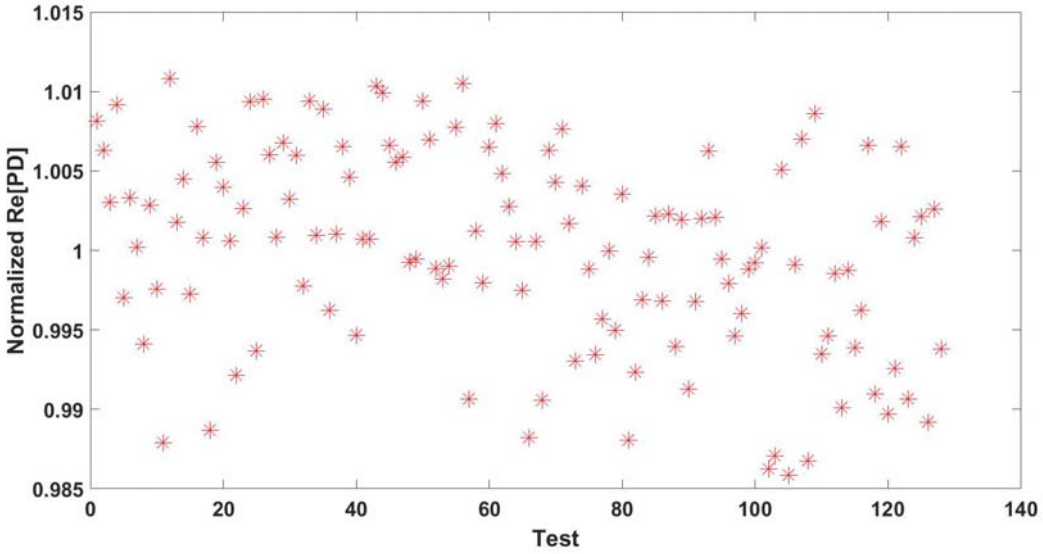


(b)

Figure 4.7 System repeatability test at 10 kHz: (a) real part of potential drop (b) real part of potential drop normalized by average value



(a)



(b)

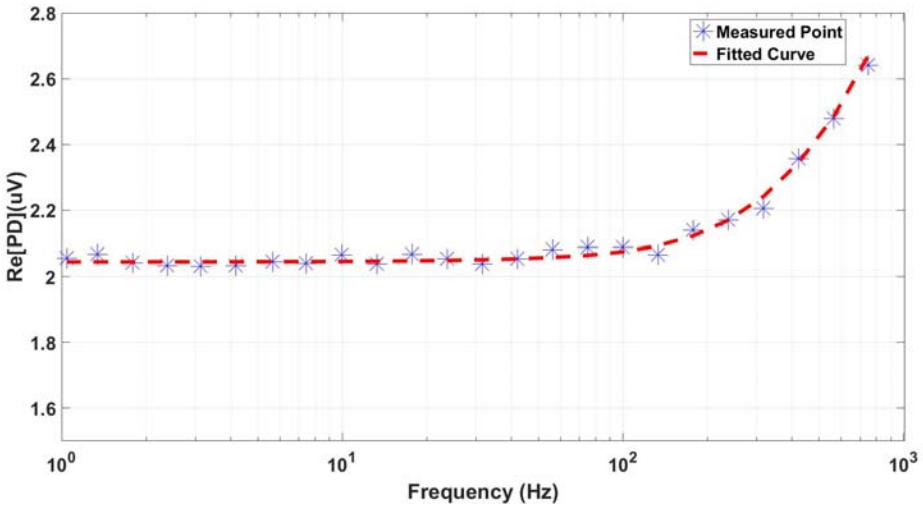
Figure 4.8 System repeatability test at 100 kHz: (a) real part of potential drop (b) real part of potential drop normalized by average value

4.4 System Accuracy Test

Previous section demonstrates the precision of this new ACPD system, and this section verifies the accuracy of it. Comparing measured conductivity and permeability with values from literature, the accuracy of this new system can be validated. Two groups of test specimens are used. Group one contains three non-ferromagnetic specimens, while group two contains three ferromagnetic specimens.

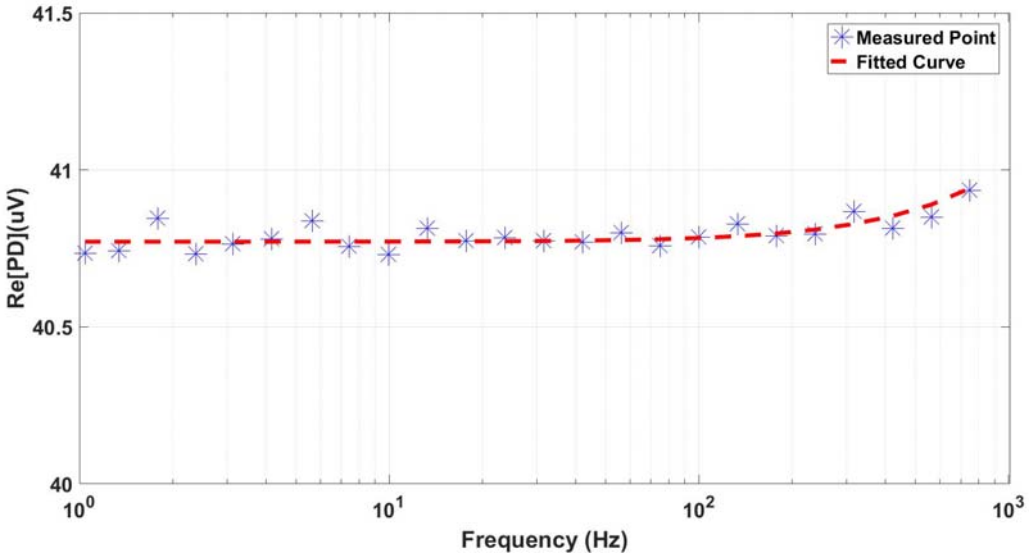
4.4.1 Experiment on non-ferromagnetic specimens

Three specimens in this group are 12 mm thick aluminum 6061-O plate, 13 mm thick 304 stainless steel plate, and 12 mm thick titanium Ti-6Al-4V plate. They represent metal with high, medium and low conductivity respectively. ACPD measurement results and curve fitting results are shown in figure 4.9. The fitted curve is from nonlinear regression based on expression 1.4. Because the plate thickness is known, the electrical conductivity of the specimen can be estimated from curve fitting.

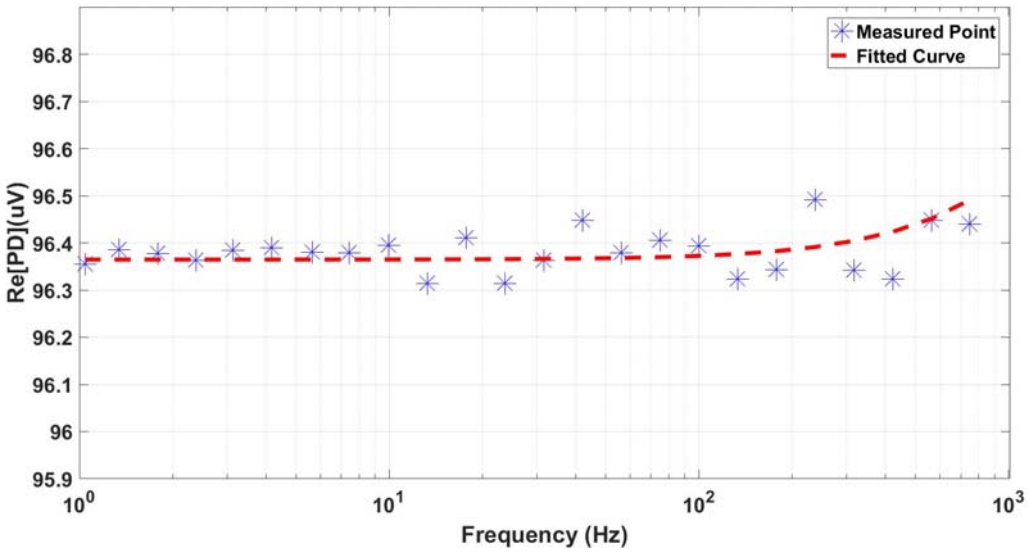


(a)

Figure 4.9 ACPD measurement and curve fitting for (a) aluminum 6061-O



(b)



(c)

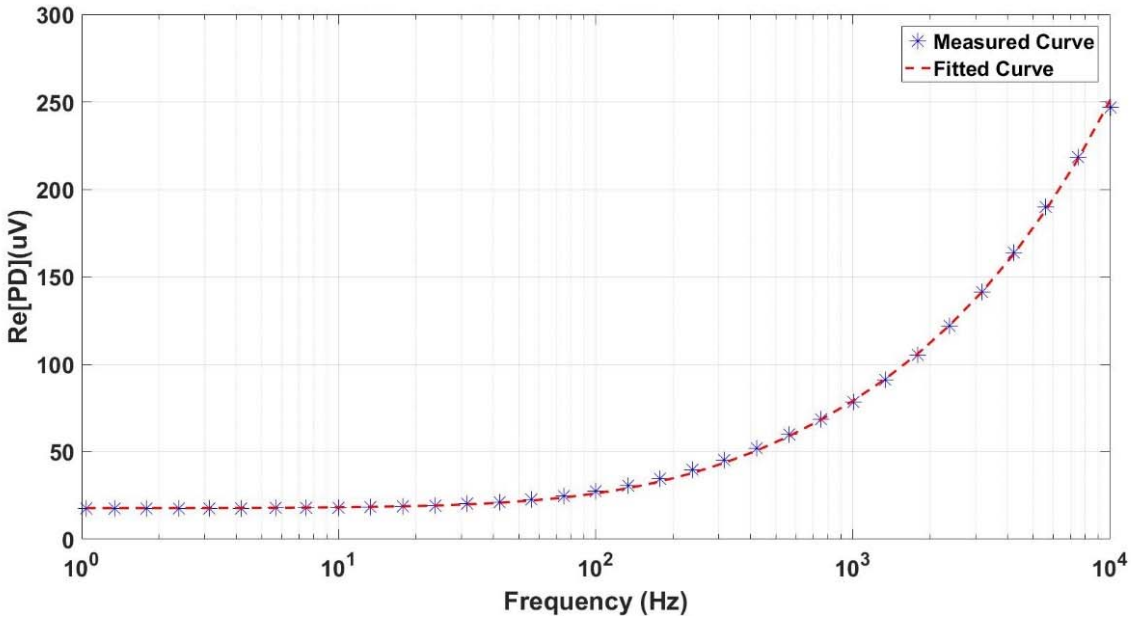
Figure 4.9(continued) (b) 304 stainless steel and (c) titanium Ti-6Al-4V

Table 4.5 Conductivity of specimen from ACPD curve fitting

Material	Conductivity(fitted)	Conductivity (literature)	Relative Error
Aluminum 6061-O	27.2 MS/m	27.3 MS/m	-0.37 %
304 stainless steel	1.36 MS/m	1.38 MS/m	-1.4 %
Titanium Ti-6Al-4V	0.556 MS/m	0.561 MS/m	-0.89 %

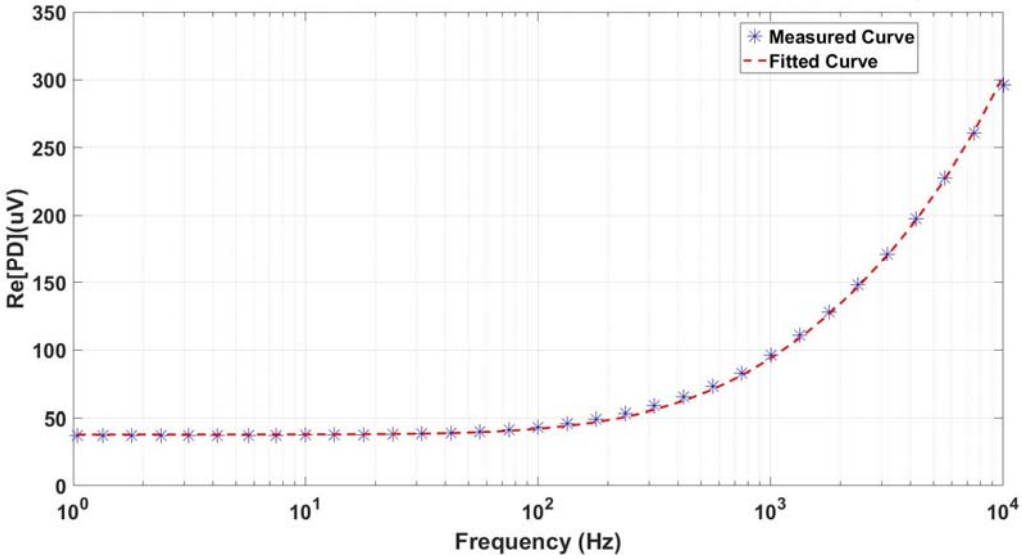
4.4.2 Experiment on ferromagnetic specimens

Three specimens in this group are 25 mm tall stainless steel cylinder, 13 mm thick stainless steel plate, and 1.27 mm thick weld steel plate. These three samples represent half space, thick plate and thin plate, respectively. Similar curve fitting is applied to the ACPD result of those specimens. Conductivity and initial permeability can be acquired from curve fitting shown below.

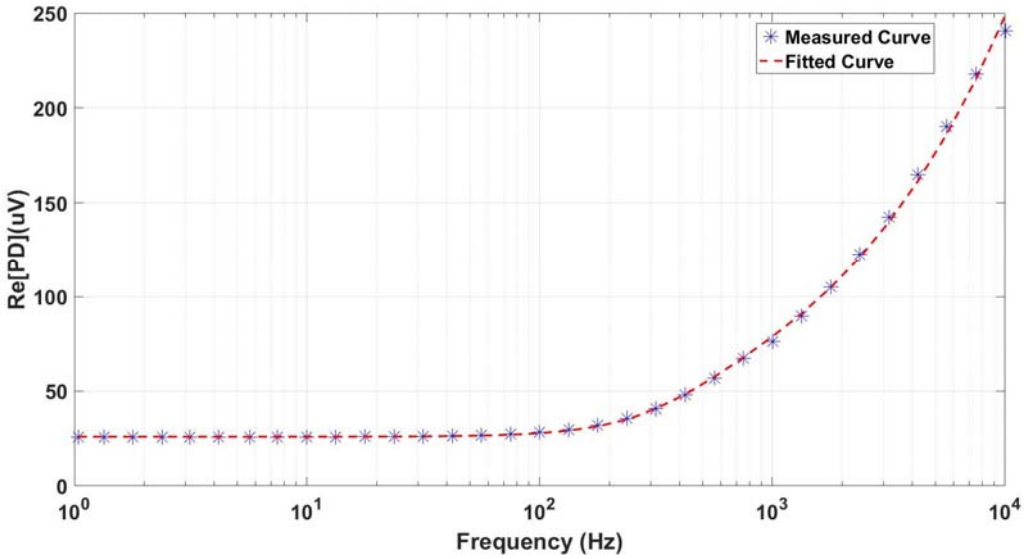


(a)

Figure 4.10 ACPD measurement and curve fitting for (a) 25 mm tall stainless steel cylinder



(b)



(c)

Figure 4.10(continued) (b) 13 mm thick stainless steel plate and (c) 1.27 mm thick weld steel plate

Table 4.6 Conductivity and Permeability Result From ACPD Curve Fitting

Sample	Relative Permeability	Conductivity
Stainless steel cylinder	94.4	2.97 MS/m
13 mm thick stainless steel plate	70.0	1.41 MS/m
1.27 mm thick weld steel plate	211	6.76 MS/m

Table 4.6 lists the estimated conductivity and relative permeability of the above three samples. Section 4.4.1 already demonstrated that the conductivity measurement is dependable. However, the accuracy of relative permeability measurement must be verified using a separate approach. One way of evaluating material permeability is inductance measurement method [51].

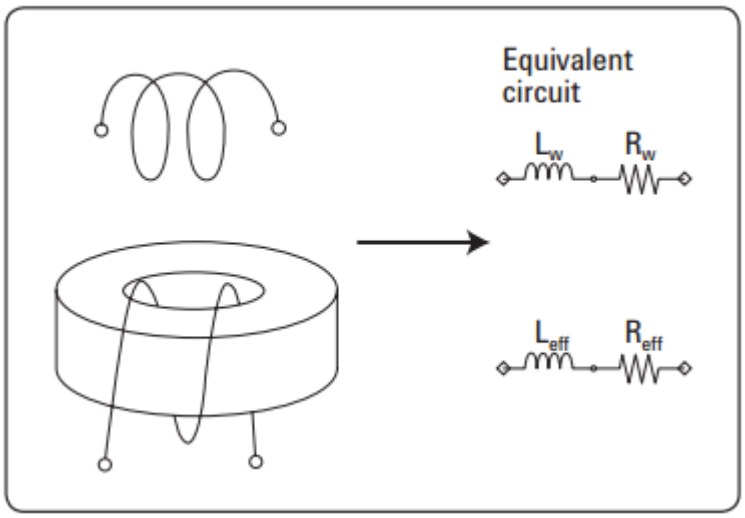


Figure 4.11 Method of measuring effective permeability [49]

As shown in Figure 4.11, the relative permeability of magnetic material can be derived from the self-inductance of a cored inductor. Yet this simple approach is not feasible for these three samples. To solve this problem, this thesis propose a time domain method to verify the relative permeability measurement result from ACPD. This time domain method is the main topic of next chapter. Time

domain potential drop calculation can be carried out using parameters listed in Table 4.6, then the time domain measurement is performed using the exact same configuration as in ACPD measurement, finally comparing the theoretical calculation and experimental result shall lead to the conclusion regarding the accuracy of ACPD permeability measurement. Another indirect way of verifying ACPD permeability measurement is to use eddy current test technique.

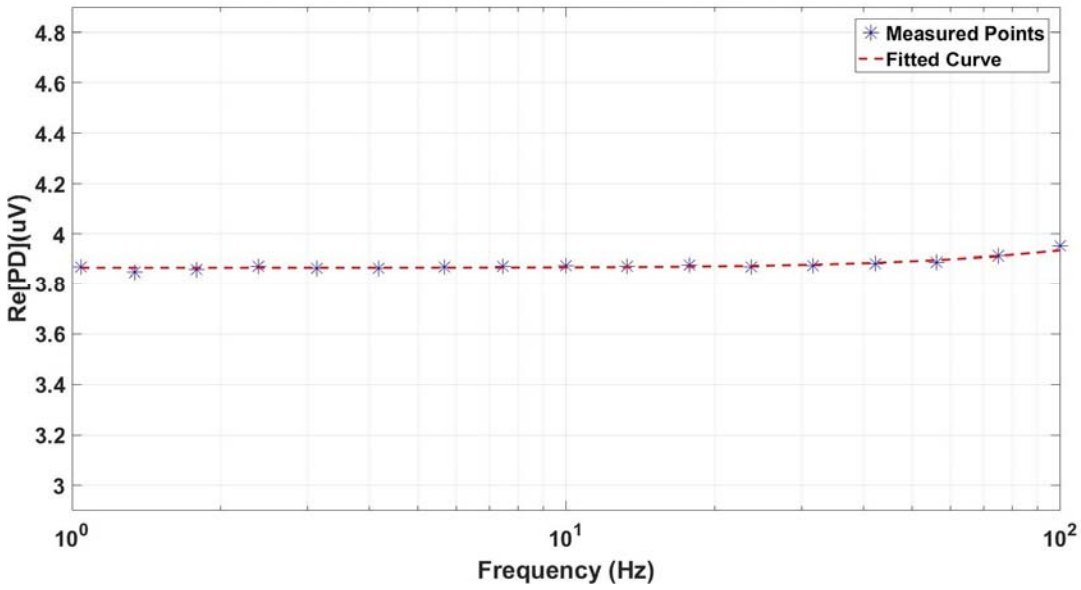
4.5 ACPD For Material Characterization

This section demonstrates the capability of ACPD for case depth measurement and non-destructive hardness profile measurement.

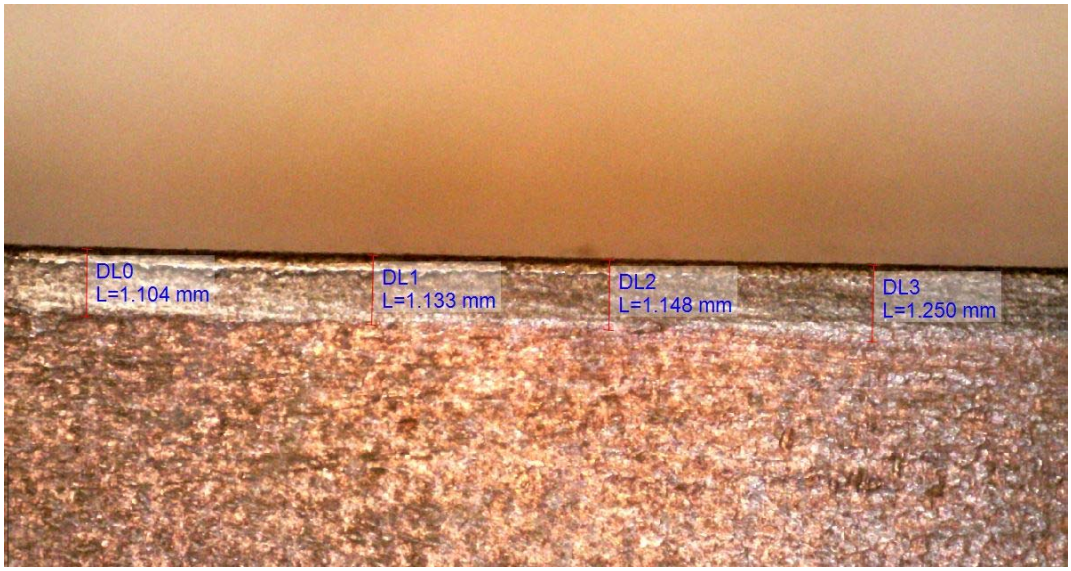
Figure 4.12 Titanium clad copper bar

Figure 4.12 shows a copper bar coated with a layer of titanium for enhanced resistance to corrosion. ACPD measurement is performed from 1 Hz to 100 Hz using 3 mm pin separation probe. Using the same nonlinear regression routine in Matlab and expression 1.8, the coating thickness can be

acquired. The estimated coating thickness is 1.15 mm, which has a 1% error compared with average measured thickness in Figure 4.12(b)



(a)



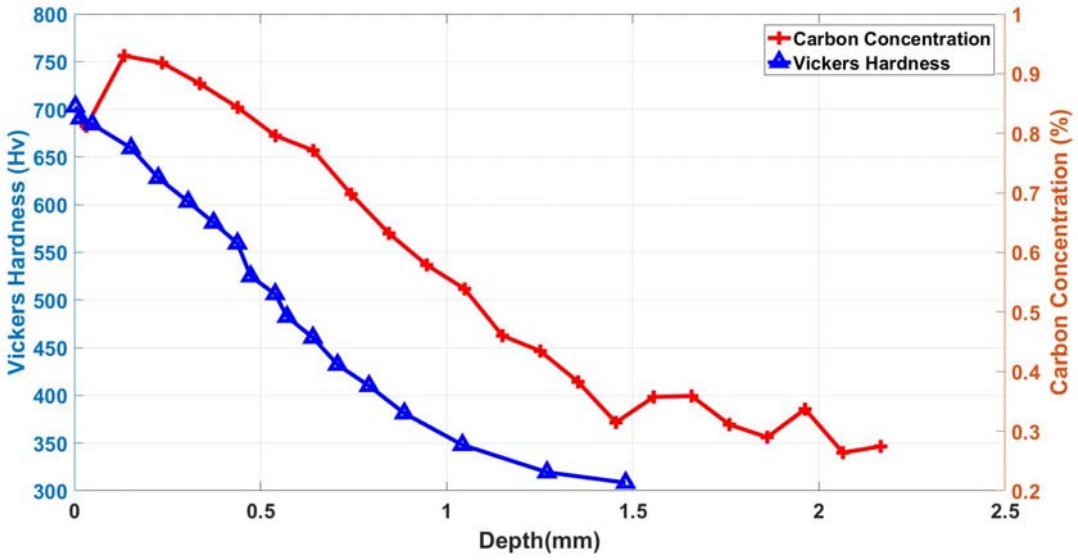
(b)

Figure 4.12 (a) Titanium clad copper bar ACPD measurement result and (b) average coating thickness using microscope is 1.16 mm

This experiment demonstrates that ACPD can be used to evaluate coating thickness and APS1006 is able to provide high quality data for this application.

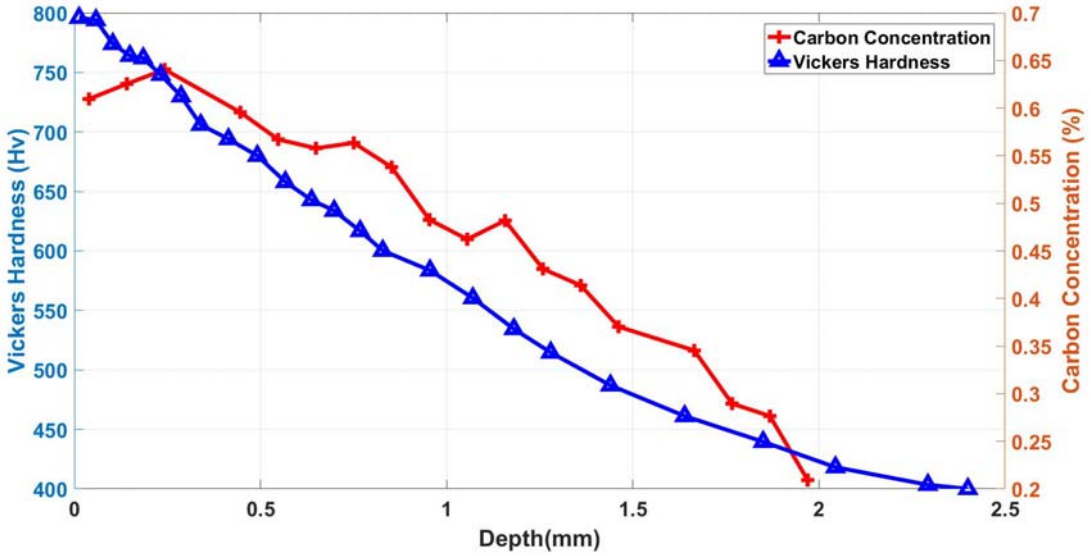
A more interesting application of ACPD is to evaluate hardness profile of a hardened steel non-destructively. Figure 4.13 shows two such specimens.

Figure 4.13 Hardened steel specimen 8002 and 8055



(a)

Figure 4.15 Carbon concentration and hardness for specimen (a) 8002



(b)

Figure 4.15(continued) and (b) 8055

Please note that the hardness profile in Figure 4.15 is acquired by destructive method. Hardness profile measurement is of very high industrial value because it is an important step for quality assurance for a variate of mechanical components, such as bearings, gears and shafts. Case hardened components has better resistance to wear. Destructively evaluate every components is not realistic, thus different nondestructive evaluation methods have been developed for such application, such as resonant acoustic method[52], Barkhausen noise measurement [53] and eddy current measurement[54]. Since ACPD technique measures electrical properties of specimen under test, the correlation between electrical properties and hardness must be established. The case hardening procedure reduces the conductivity and permeability of hardened region, and the electrical conductivity change tracks hardness changes fairly well [55].

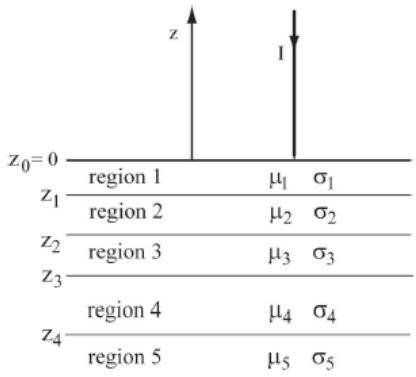


Figure 4.16 Specimen modeled as layered conductive plate

The case hardened specimen 8002 and 8055 can be modeled as layered conductive plates with linearly changing conductivity and permeability with respect to depth as shown in Figure 4.17.

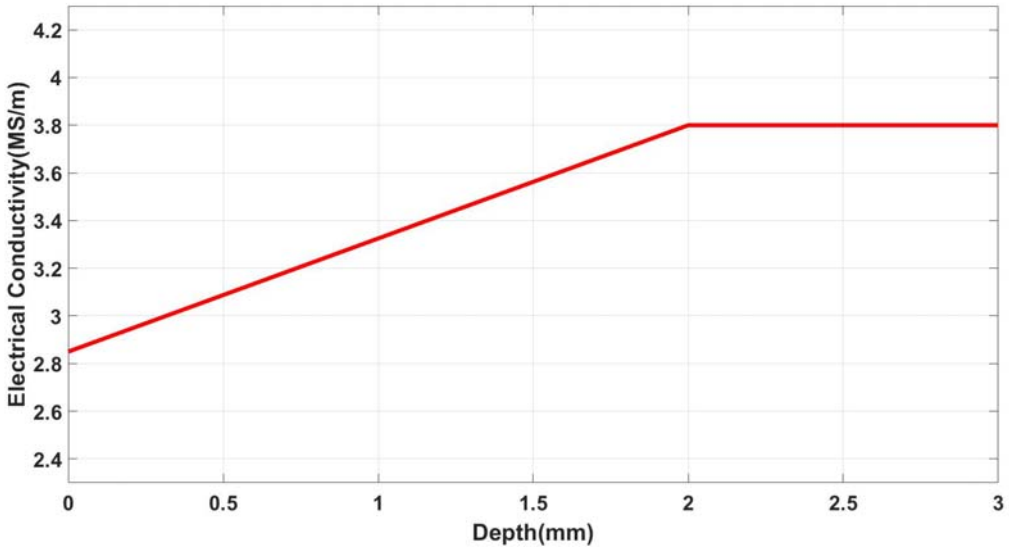


Figure 4.17 Linear model for conductivity and permeability assuming hardened layer thickness D is 2.0 mm

The conductivity and permeability linearly increase with respect to depth until the depth reaches hardened layer thickness D, where those two parameters level off to substrate conductivity and permeability.

The forward problem of layered conductive plate has been solved by Professor John.R.Bowler at CNDE in Iowa State University. Given the forward problem solution, as well as surface electrical properties, case depth and substrate electrical properties, the response from ACPD measurement can be calculated. To solve the inverse problem, an algorithm is developed which can be summarized in Table 4.7

Table 4.7 Inverse Algorithm for Hardness Profile Evaluation

Step	Operation	Output
1	ACPD measurement on substrate material	Conductivity and permeability of substrate material
2	ACPD measurement on specimen surface	Response of layered structure
3	Traverse all possible D and use curve fitting to find out surface conductivity and permeability for each given D. Each of those curve fitting have a fitting error associated with it, and thus the D with minimum fitting error is the most possible hardened layer depth.	Estimated hardened layer depth D.

In reality, the substrate properties can be measured before hardening procedure. However in this experiment, the specimens were sent to us after hardening, thus substrate material must be exposed by removing part of the specimen material as shown in Figure 4.13. The cross section available for substrate measurement is relatively narrow(12 mm), and 1.5 mm pin separation probe must be used to avoid edge effect.

For specimen 8002, the procedure can be demonstrated from Figure 4.18 to Figure 4.20.

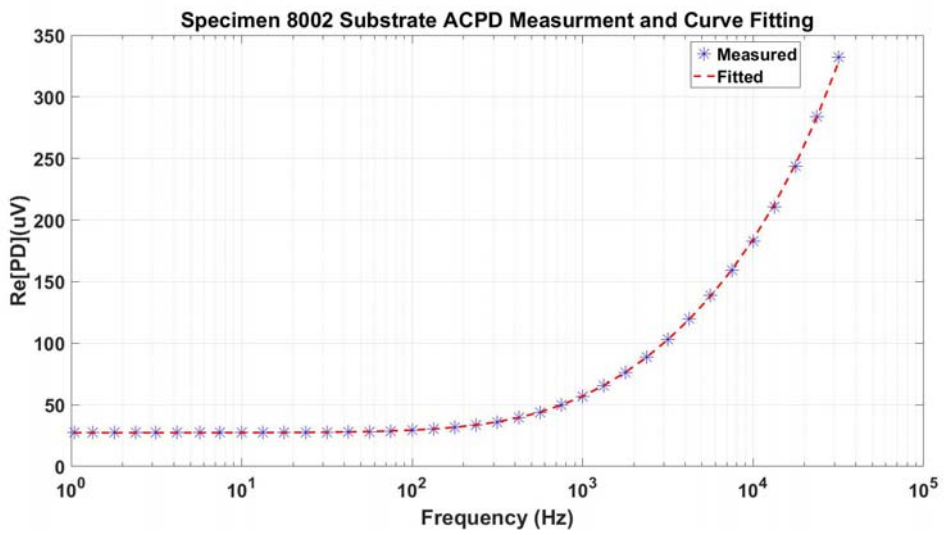
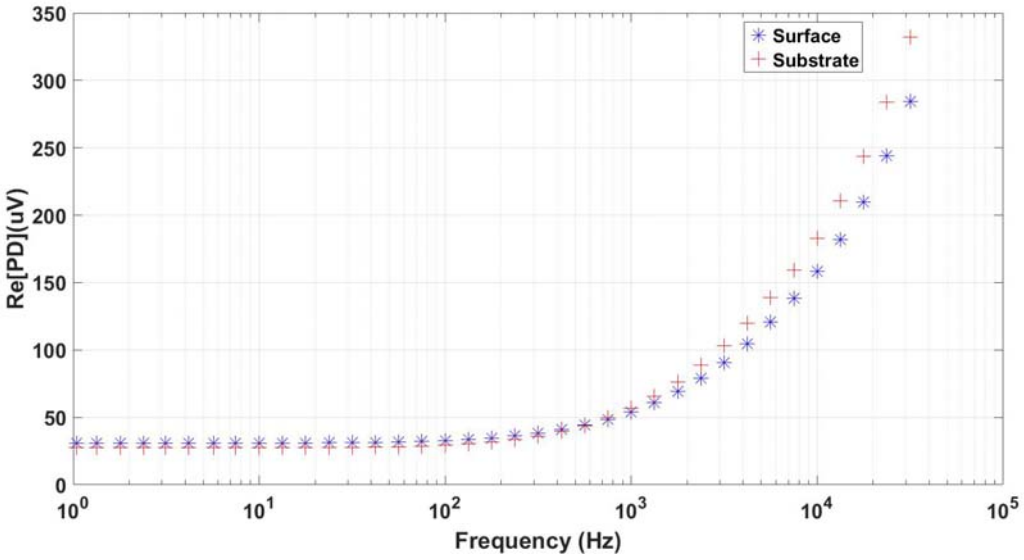
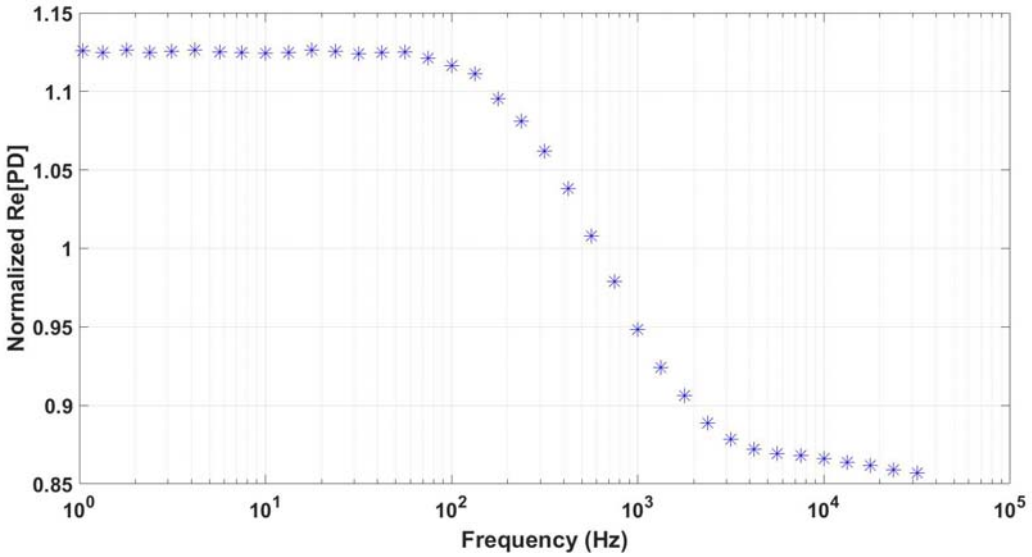


Figure 4.18. Step 1:The fitted conductivity and permeability for specimen 8002 substrate are 3.81 MS/m and 70.5, respectively.



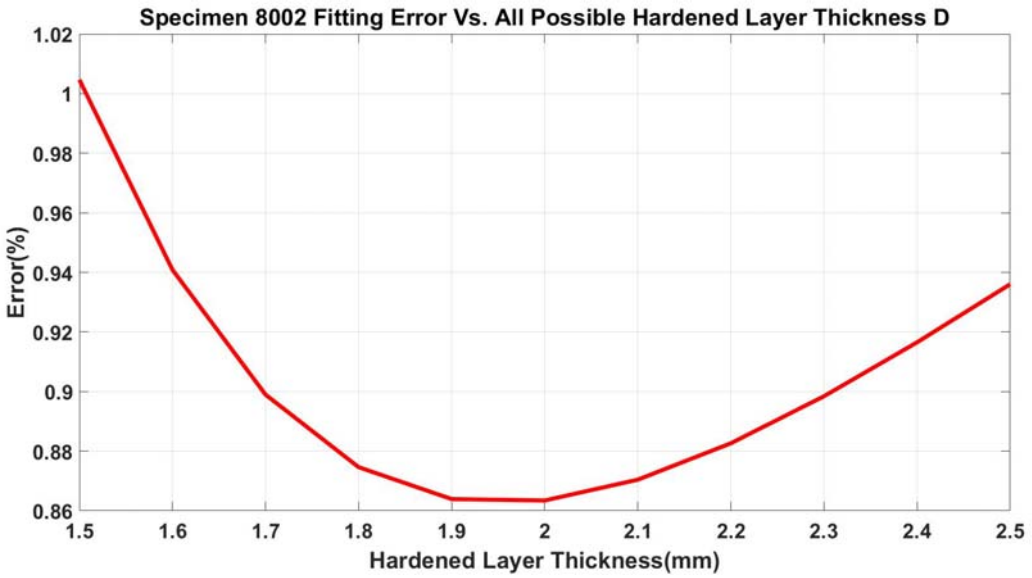
(a)

Figure 4.19. Step 2: (a) surface real part of potential drop



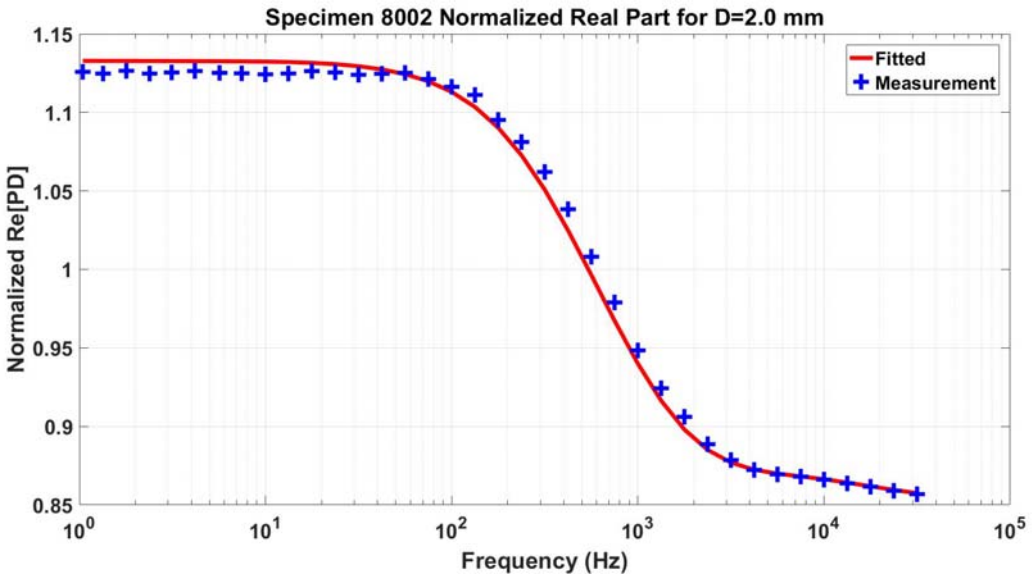
(b)

Figure 4.19(continued) (b) surface real part of potential drop normalized by substrate counterpart



(a)

Figure 4.20. Step 3: (a) Most possible D is 2.0 mm



(b)

Figure 4.20(continued) (b) The fitted surface conductivity and permeability are 3.01 MS/m and 40.6, respectively.

Similar procedure can be applied to specimen 8055 and Table 4.8 summarizes the results from the two specimens.

Table 4.8 Estimated Material Properties and Hardened Layer Thickness

	Specimen 8002	Specimen 8055
Surface Conductivity	3.01 MS/m	2.71 MS/m
Substrate Conductivity	3.81 MS/m	3.84 MS/m
Surface Relative Permeability	40.6	39.3
Substrate Relative Permeability	70.5	70.6
Estimated Hardened Layer Thickness	2.0 mm	2.5 mm

Compare estimated hardened layer thickness with destructive result in Figure 4.15, it can be concluded that ACPD measurement is able to evaluate hardness profile with reasonably good accuracy.

4.6 Conclusion

This chapter discusses the testing and verification of ACPD system. The system repeatability is exceptional for frequency from 1 Hz up to 10 KHz. Future works must be focused on improving the system noise performance from 10 KHz and above. Because of the special sampling approach discussed in Chapter 3, the system measurement speed is far superior to any other ACPD lab systems ever built. This system is able to cover 1 Hz to 100 KHz within 14.6 seconds. The accuracy of low frequency result or conductivity measurement is fully verified. For high frequency part, Chapter 5 proposes a time domain method to independently verify the relative permeability result from ACPD measurement. This ACPD system can also be used in coating thickness evaluation and hardened layer thickness evaluation.

CHAPTER 5. TRANSIENT POTENTIAL DROP MEASUREMENT

5.1 Introduction

Transient potential drop measurement is the time domain version of ACPD. The drive current is no longer an AC signal at certain frequency, but an exponentially rise pulse signal as shown in Figure 5.1.

$$I(t) = 1 - \exp(\frac{-t}{\tau}) \quad (5\text{-}1)$$

where τ is time constant

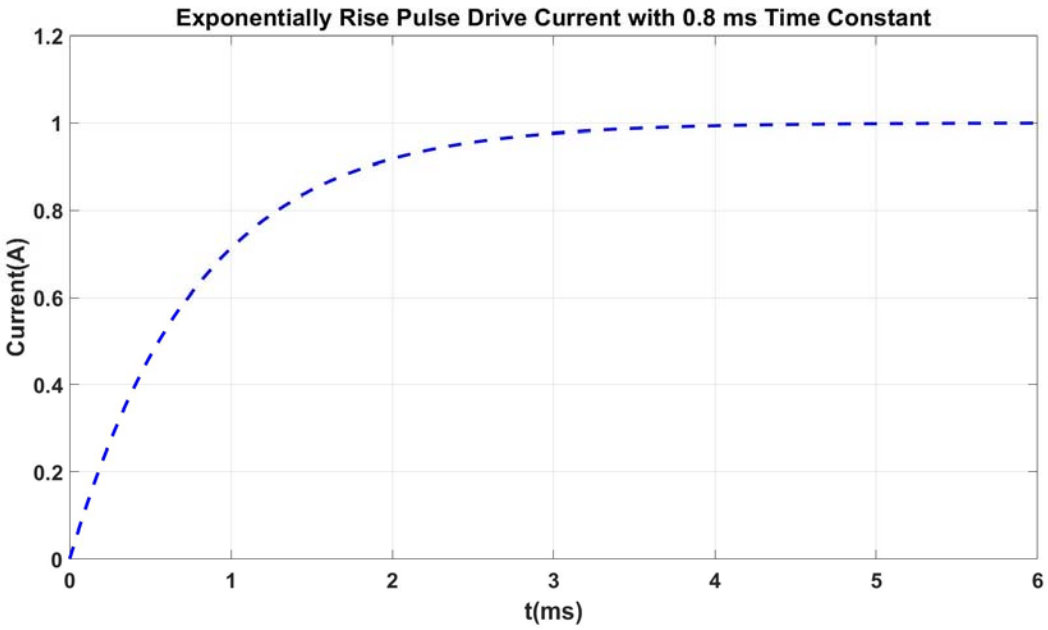


Figure 5.1 Typical drive current for transient potential drop measurement

Similarly, instead of being a complex phasor, the final output of transient drop measurement is a time domain response. Reference [56] discusses the main approach to model transient potential drop, which uses the Laplace transform to obtain the time domain response from ACPD model.

For homogeneous half space, the step up response can be expressed as [56]:

$$f_0(\rho,t)=\frac{1}{\rho}\mathrm{erfc}(\sqrt{\frac{\mu\sigma}{4t}}\rho)-\sqrt{\frac{\mu\sigma}{4\pi t}}[E_1(\frac{\mu\sigma}{4t}\rho^2)+2\log(\rho)] \tag{5-2}$$

Where ρ is pin distance shown in Figure 4.1.

For homogeneous half space, the exponential rise response can be expressed as [56]:

$$f_v(\rho,t)=\frac{v}{2\rho}[h(\kappa,v,t)-h(\kappa,-v,t)] \tag{5-3}$$

where $\kappa^2=\mu\sigma\rho^2$, $v^2=\frac{-1}{\tau^2}$ and

$$h(\kappa,v,t)=\frac{1}{v}\mathrm{erfc}(\frac{\kappa}{2\sqrt{t}})-e^{v^2t}[\frac{1}{v}e^{v\kappa}\mathrm{erfc}(v\sqrt{t}+\frac{\kappa}{2\sqrt{t}})$$

$$+\kappa\int_1^\infty\frac{1}{u}e^{v\kappa u}\mathrm{erfc}(v\sqrt{t}+\frac{\kappa u}{2\sqrt{t}})\,du+\kappa\mathrm{erfc}(v\sqrt{t})\ln\rho] \tag{5-4}$$

Figure 5.2 gives example calculations for stainless steel cylinder in section 4.4.2, which is driven by exponential rise pulse current with different time constant.

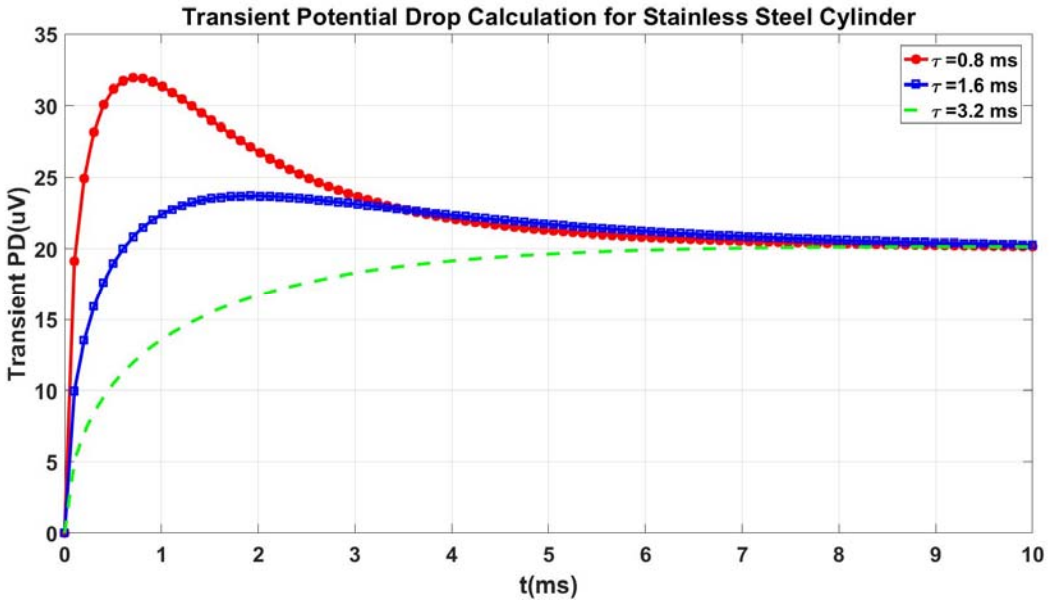
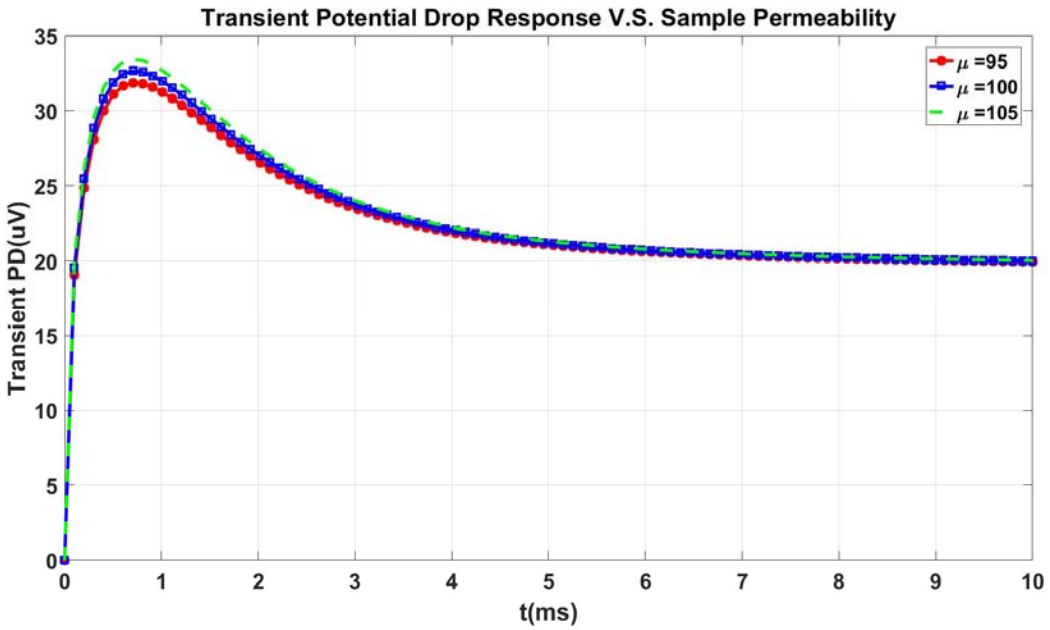
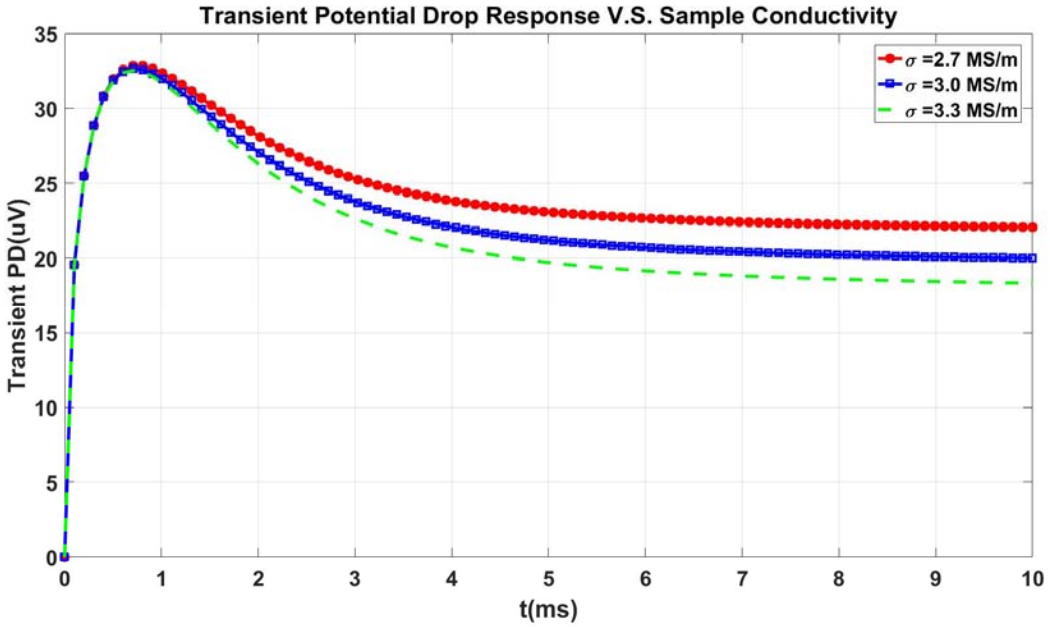


Figure 5.2 Transient potential drop for different drive current time constant



(a)



(b)

Figure 5.3 (a) Transient potential drop for different relative permeability and (b) Transient potential drop for different conductivity

Figure 5.3 illustrates a very interesting behavior of transient potential drop. For short term response, it mostly depends on relative permeability; while for long term settling value, it only depends on conductivity. For example, in Figure 5.3 (a), the peak value is largely determined by relative permeability.

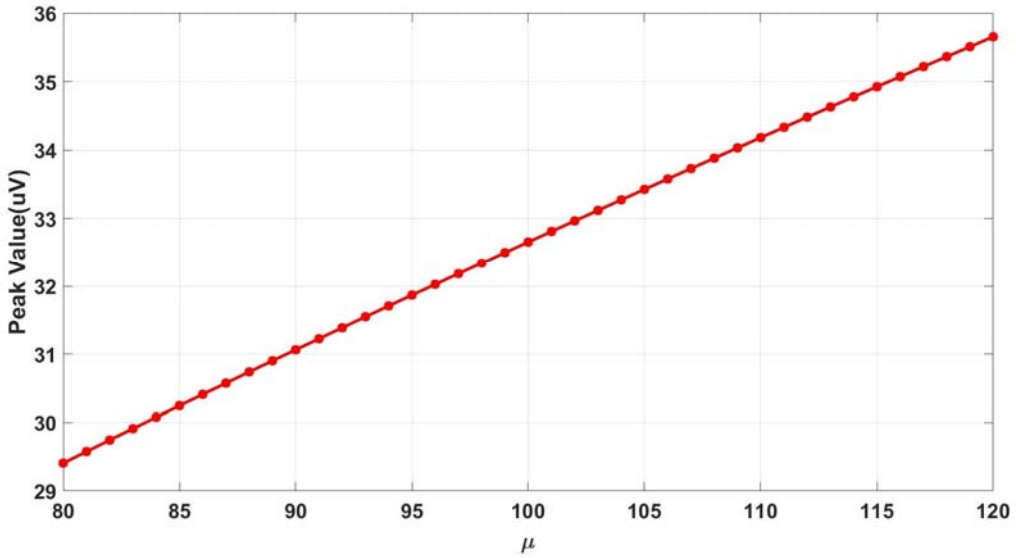


Figure 5.4 Transient potential drop peak value verses permeability

Figure 5.4 illustrates that the peak value can be used to infer sample permeability as they have a simple linear relationship.

This chapter will take advantage of the capability of transient potential drop measurement and verify the permeability estimation in Table 4.6. Being a broad band measurement regime, transient potential drop has relatively more electronic noise compared with ACPD system. But this drawback can be mitigated using analog filter and signal averaging.

5.2 Transient Potential Drop Measurement Setup

An arbitrary waveform generator is programmed to generate exponentially rise pulse voltage signal similar to the waveform in Figure 5.1. This drive voltage is converted into drive

current by the transconductance amplifier. The pick-up voltage is then amplified and filtered for data acquisition using oscilloscope.

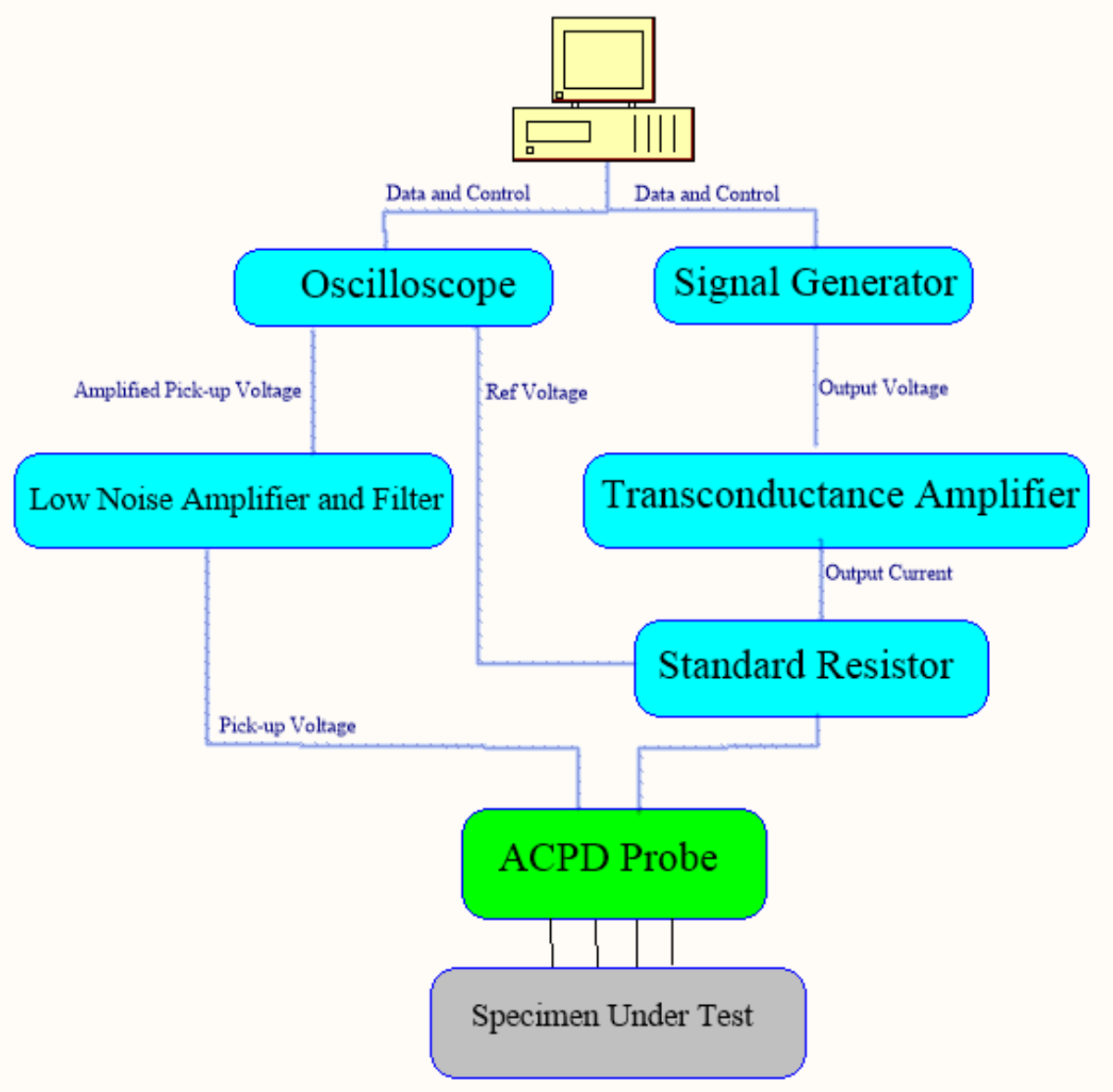


Figure 5.5 Block diagram of transient potential drop measurement system.

Please note that the waveform has been averaged by 16 times, which effectively reduces noise. Blue line is the amplified pick-up voltage and red line is drive current.

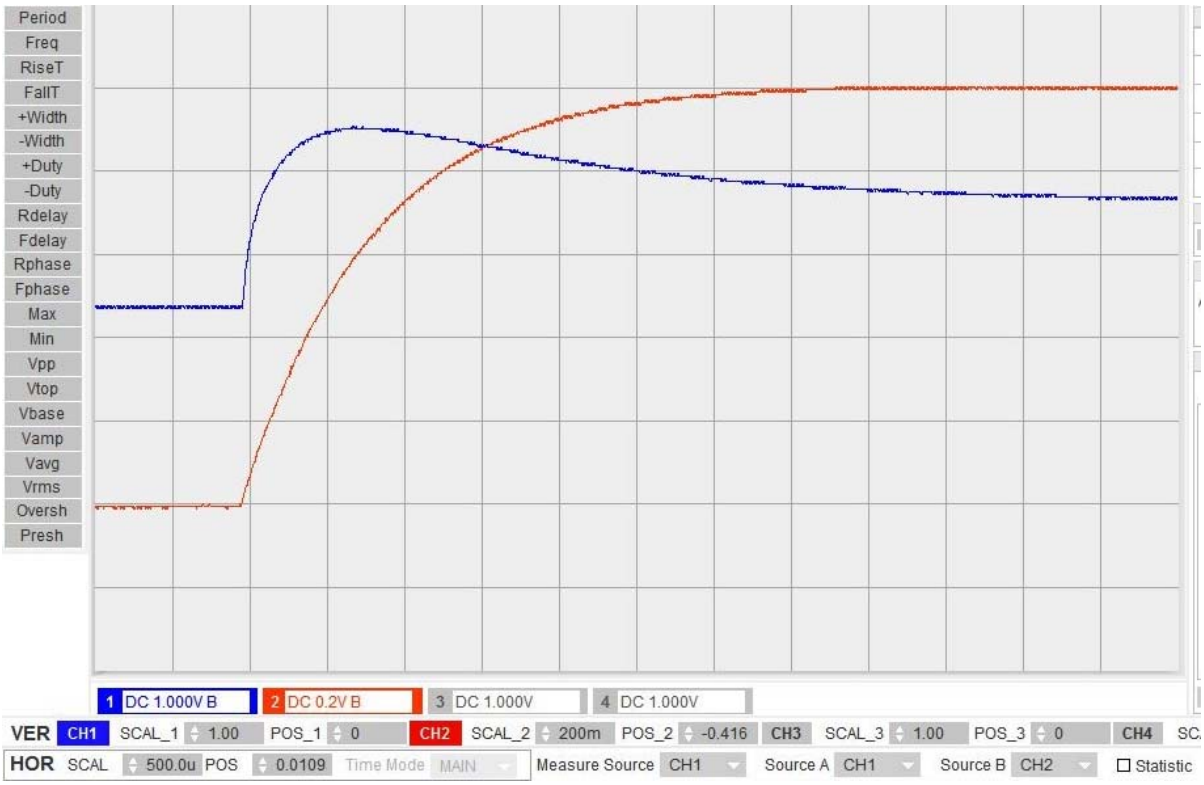


Figure 5.6 Drive current and transient potential drop response captured by oscilloscope

5.3 Low Pass Filter Characterization

As mentioned in the above sections, low pass filter is an indispensable part of the signal chain. In order to compare measured transient drop response and theoretical calculation quantitatively, the low pass filter must be fully characterized. Zurich Instruments MFLI lock-in amplifier is used to measure the normalized transfer function of the low pass filter as shown in Figure 5.7

Use nonlinear regression, the filter's transfer function can be expressed as:

$$\mathrm{TF}(s) = \frac{6.9}{(\frac{s}{2\pi 15000})^4 + 5.3(\frac{s}{2\pi 15000})^3 + 12.2(\frac{s}{2\pi 15000})^2 + 14.1\frac{s}{2\pi 15000} + 6.9} \qquad (5\text{-}5)$$

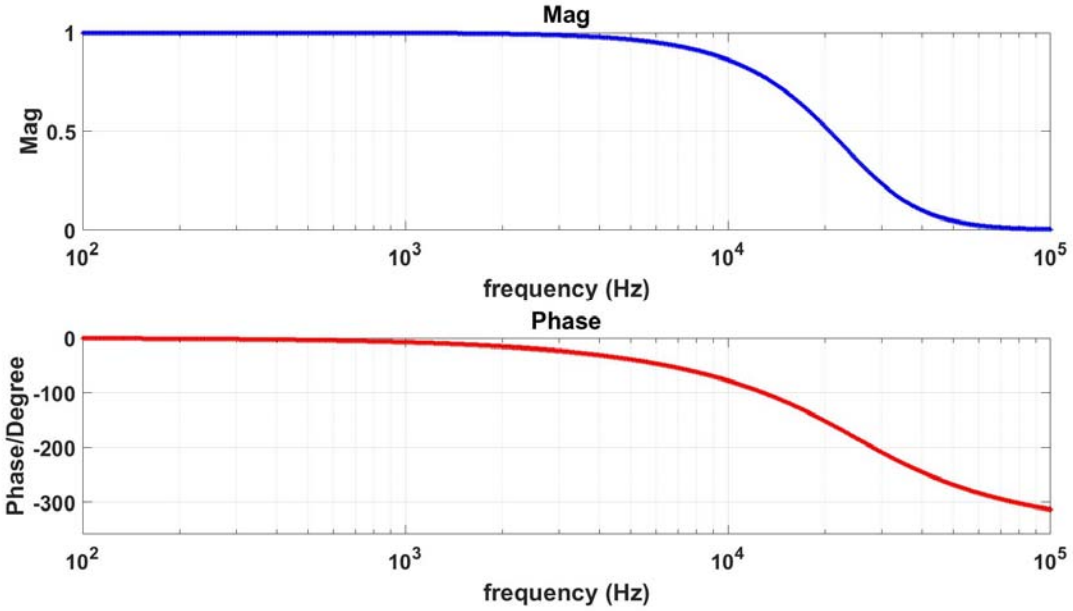
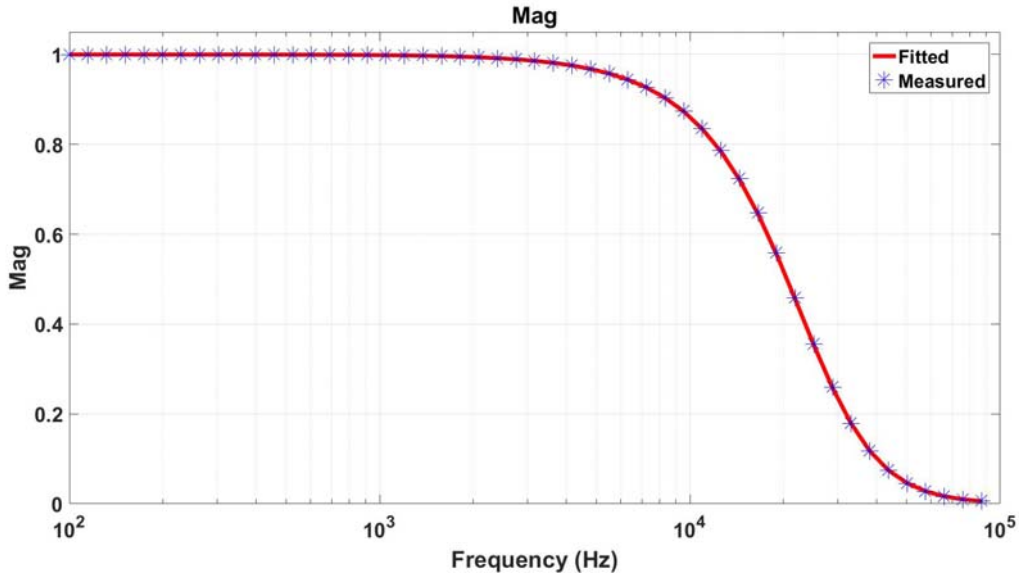
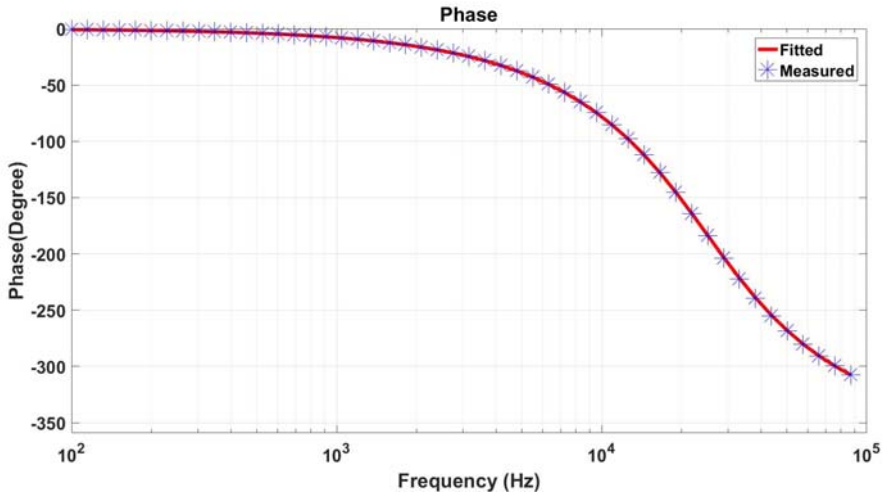


Figure 5.7 Transfer function of 15 KHz bandwidth 4th order Bessel low pass filter



(a)

Figure 5.8 Magnitude (a) for low pass filter transfer function



(b)

Figure 5.8(continued) and phase (b) for low pass filter transfer function

5.4 Numerical Laplace Inversion

Reference [56] gives analytical transient potential drop solution for homogeneous half space. For finite thickness plate and half space, numerical inverse Laplace transform routines are developed respectively. The routines are based on the Talbot algorithm [57].

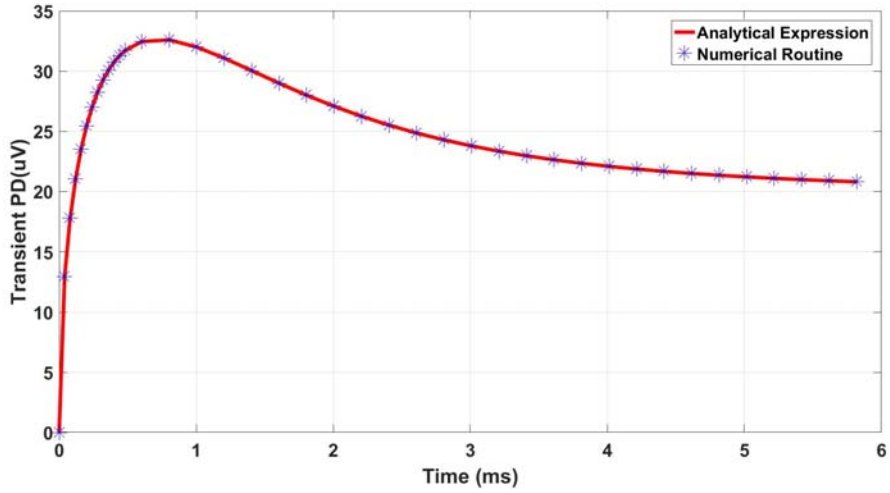


Figure 5.9 Comparison of analytical and numerical Laplace inversion for half space

Expression (5-3) is used to validate the numerical inverse Laplace transform. As seen in Figure 5.9, this numerical routine is very accurate. Similarly, with the help of expression 1.5, a numerical routine for finite thickness plate is developed. Figure 5.10 compares the finite thickness plate response with analytical expression for half-space. As the thickness increases, the plate response converges to half space response.

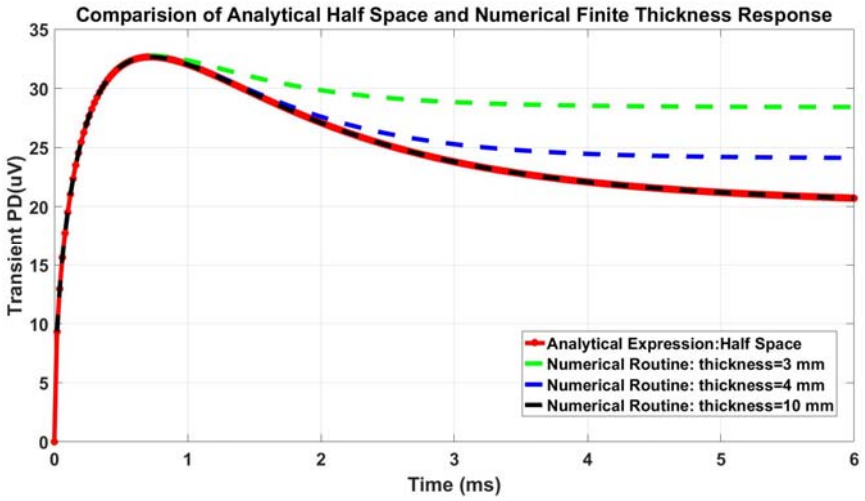


Figure 5.10 Finite thickness plate numerical routine V.S. analytical expression

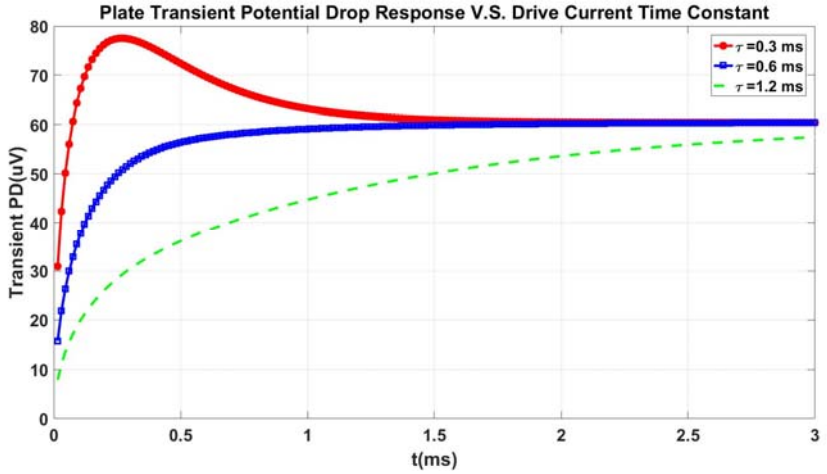
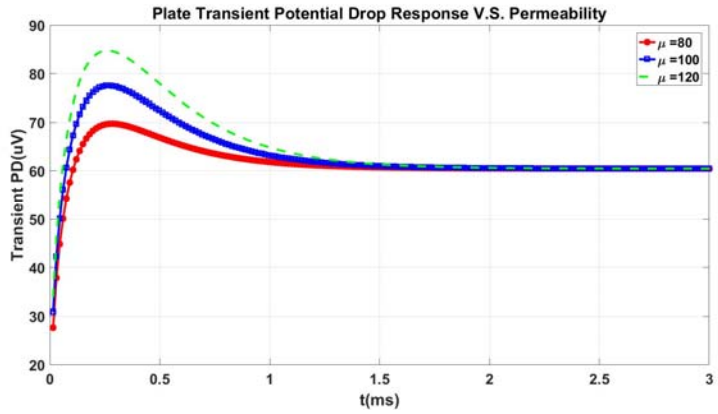
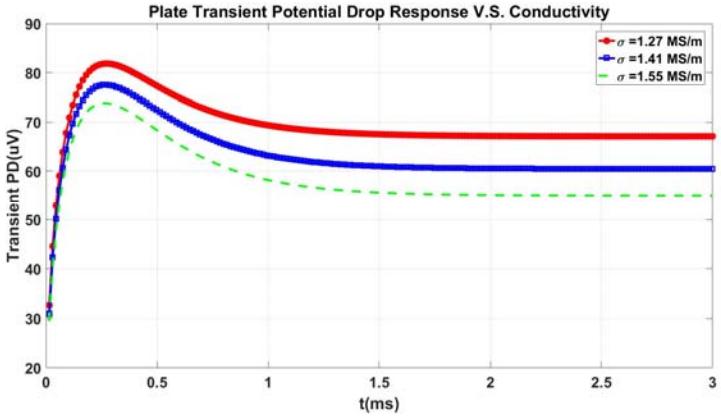


Figure 5.11 Finite thickness plate transient potential drop for different drive current time constant



(a)



(b)

Figure 5.12 (a) Finite thickness plate transient potential drop for different relative permeability and (b) Finite thickness plate transient potential drop for different conductivity

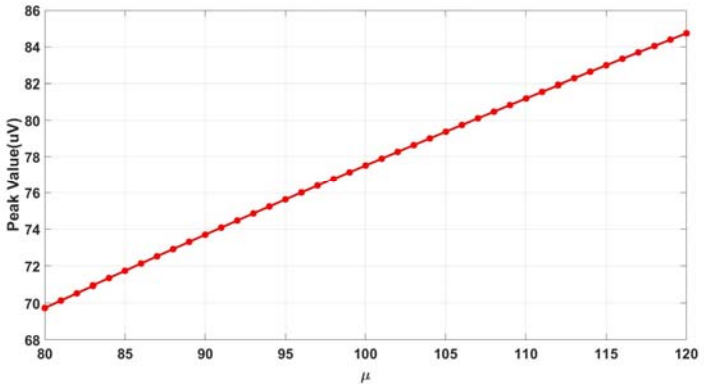


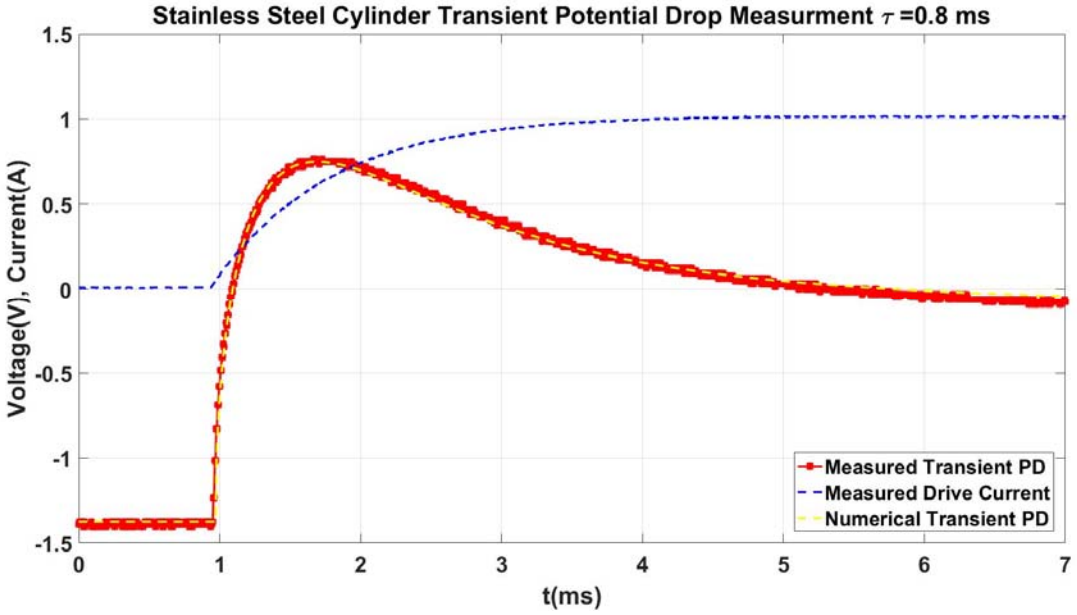
Figure 5.13 Finite thickness plate transient potential drop peak value verses permeability

From Figure 5.11, Figure 5.12 and Figure 5.13, it can be concluded that the behavior of transient potential drop for finite thickness is similar to that of half space.

5.5 Transient Potential Drop Measurement

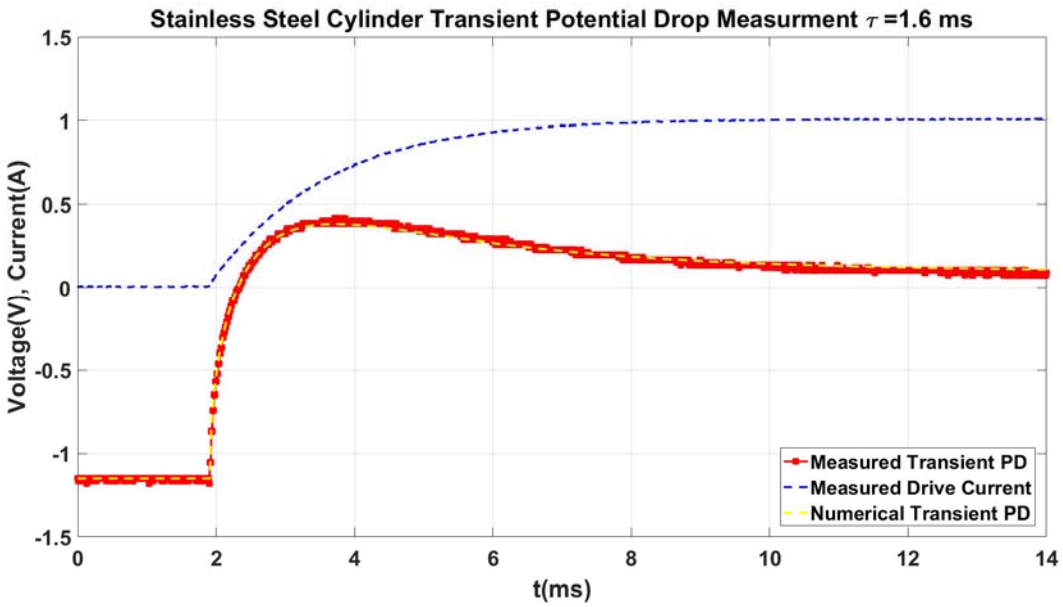
Transient potential drop measurement are performed on the three ferromagnetic samples in section 4.4.2 and the goal is to compare the measured transient data against numerical prediction using the conductivity and permeability in Table 4.6. If two sets of data match, then the conductivity and permeability in Table 4.6 is validated.

5.5.1 25 mm tall stainless steel cylinder

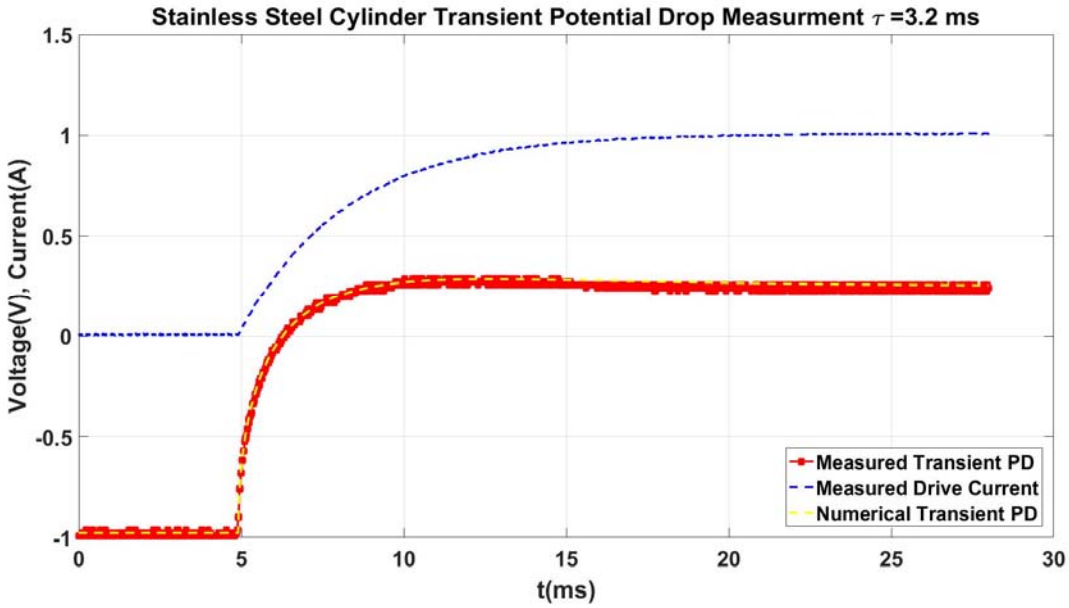


(a)

Figure 5.14 Stainless steel cylinder transient potential drop measurement for (a) τ=0.8 ms



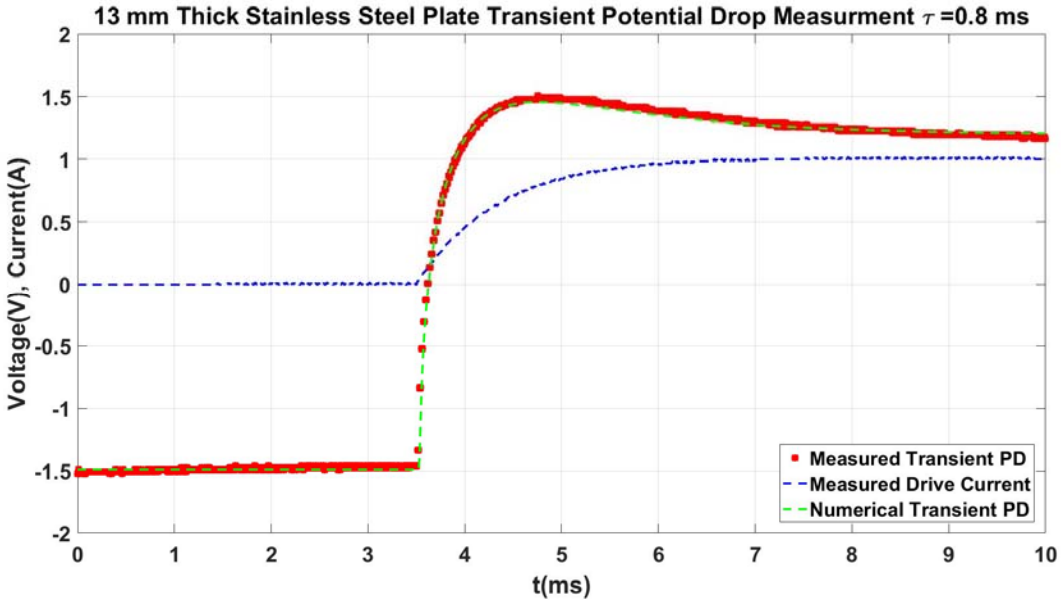
(b)



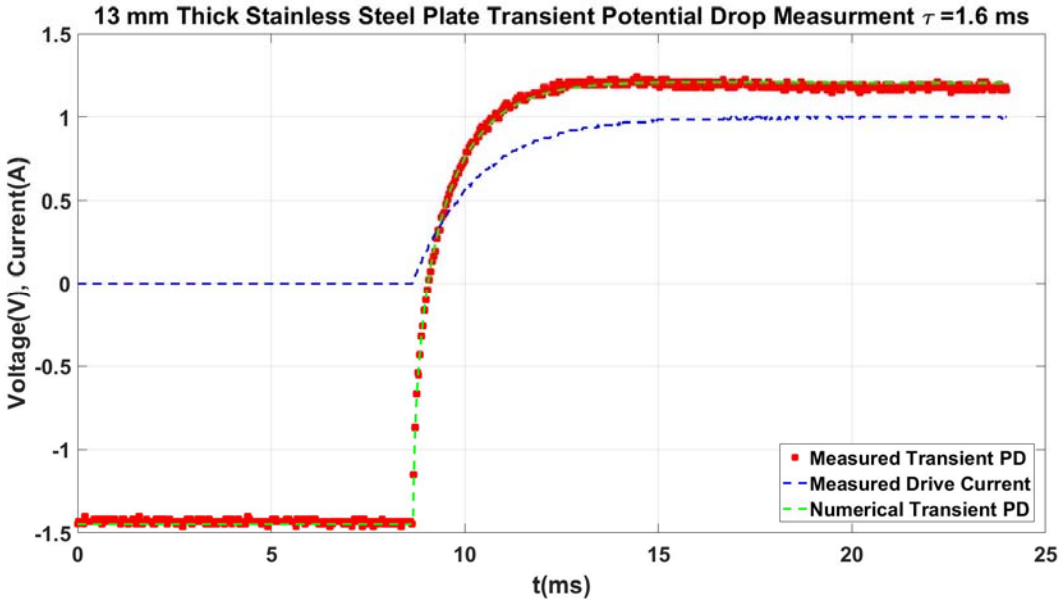
(c)

Figure 5.14 (continued) (b) τ=1.6 ms (c) τ=3.2 ms

5.5.2 13 mm thick stainless steel plate

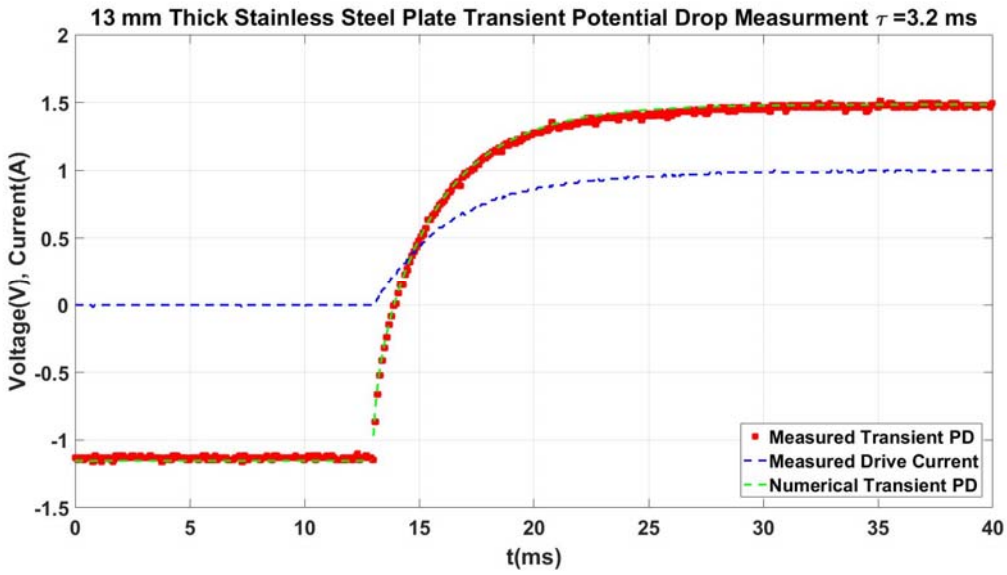


(a)



(b)

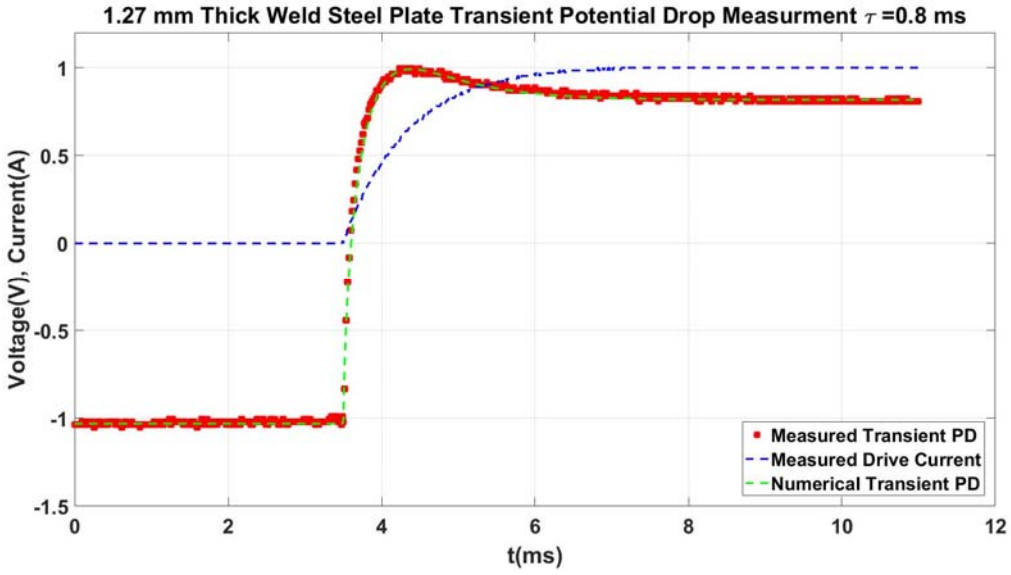
Figure 5.15 13 mm thick stainless steel plate transient potential drop measurement for (a) τ=0.8 ms (b) τ=1.6 ms



(c)

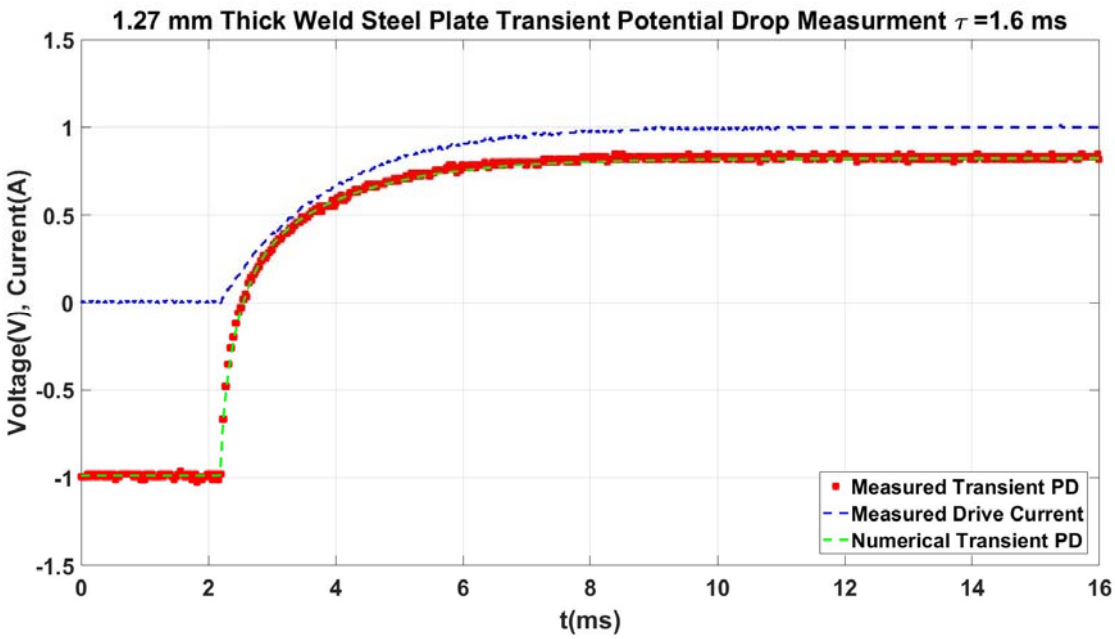
Figure 5.15 (continued) and (c) τ=3.2 ms

5.5.3 1.27 mm thick weld steel plate

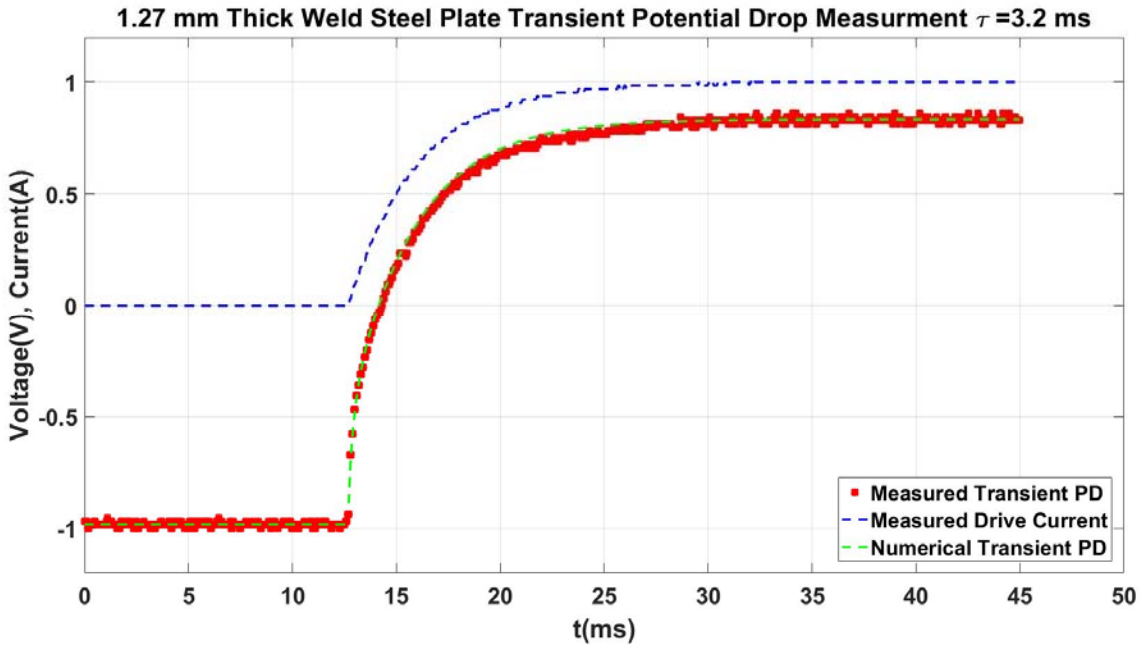


(a)

Figure 5.16 1.27 mm thick weld steel plate transient potential drop measurement for (a) τ=0.8 ms



(b)



(c)

Figure 5.16 (continued) (b) τ=1.6 ms (c) τ=3.2 ms

5.5.4 Summary

Figure 5.14, Figure 5.15 and Figure 5.16 demonstrate that numerical predications agree with measured transient potential drop data, which means that the conductivity and permeability in Table 4.6 is valid. At this point, the performance this new ACPD measurement system has been fully validated.

5.6 Conclusion

This chapter proposes using transient potential drop measurement to verify the conductivity and permeability extracted from ACPD data. To this end, numerical inverse Laplace routines are developed for half space and finite thickness plate. The numerical routine agrees with analytical solution as well as actual measurement data. Additionally, to achieve good agreement between two sets of data, the low pass filter is accurately characterized. This chapter also demonstrates that transient potential drop is a swift and accurate method to extract material conductivity and permeability. Conductivity and permeability can be "decoupled" by inspecting short term response and long term response, respectively. The advantage of such transient potential method is its simplicity, low cost and low overall system power consumption, which is attractive for structure health monitoring.

CHAPTER 6. PRECISION IMPEDANCE ANALYZER

6.1 Introduction

When an AC current flows in a coil in close proximity to a conducting surface the magnetic field of the coil will induce eddy currents in that surface. The magnitude and phase of the eddy currents affect the loading of the coil. If a crack exist in the surface under the coil, this crack will interrupt the eddy current flow, thus decreasing the loading on the coil and increasing its effective impedance. Figure 6.1 illustrates this basic configuration.

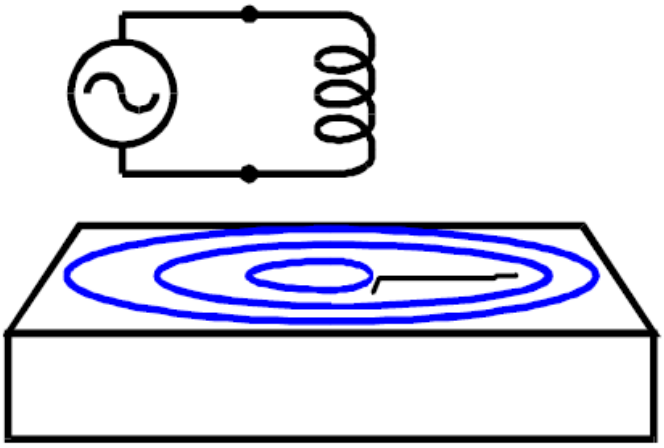
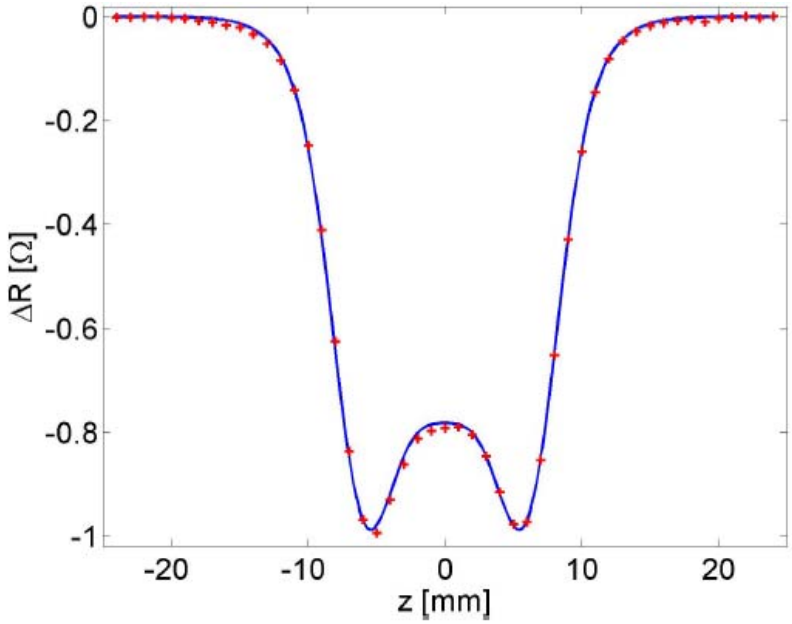
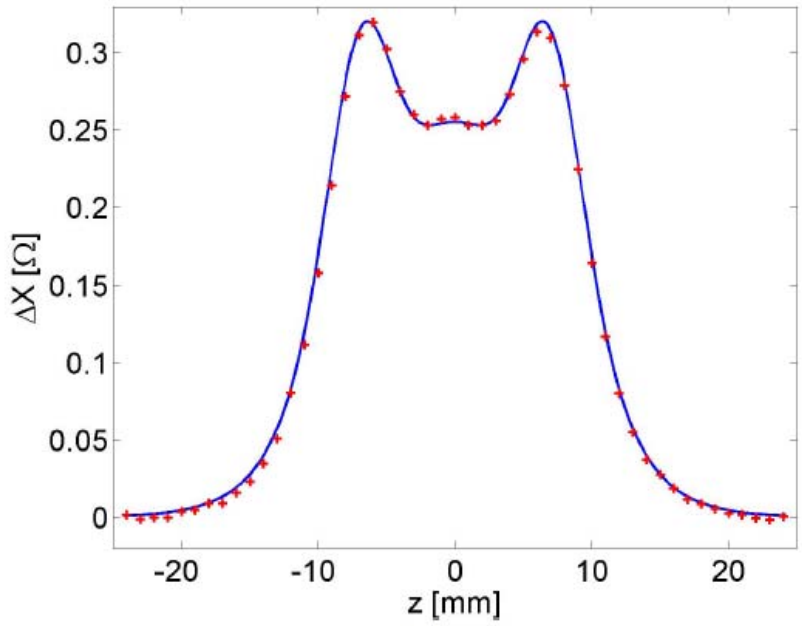


Figure 6.1 Basic eddy current testing of surface crack

If the crack is small, the impedance change caused by this crack might be very small as well. Figure 6.2 gives an experimental data of the impedance change of a pancake coil in an Inconel tube due to a longitudinal through-wall notch.



(a)



(b)

Figure 6.2 Small impedance change example (a) real part and (b) imaginary part

Precision impedance analyzer must be used to ensure the quality of the impedance data. But this chapter propose a simple but powerful impedance analyzer circuit based on precision lock-in amplifier.

6.2 Impedance Analyzer Design

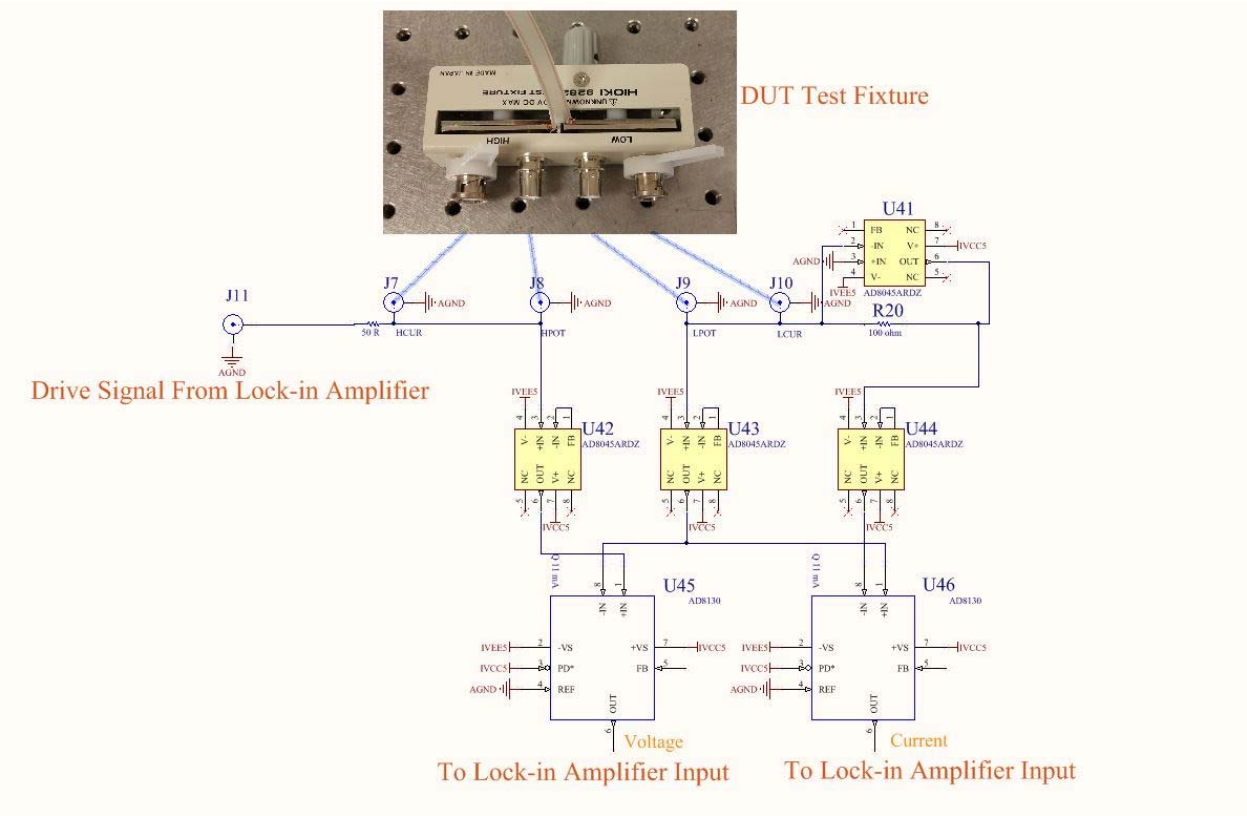


Figure 6.3 Simplified system schematic

The principle of this circuit can be explained by following the signal path. The drive signal at frequency of interest from lock-in amplifier output is connected to J11, thus the voltage between J8 and J9 is the voltage across DUT, which is buffered by U42 and U43. U45 is a subtracting amplifier whose output equals the DUT voltage. U41 and R20 is configured as a current to voltage converter and the voltage between J9 and right side of R20 equals the current flow through DUT divided by R20 value, which is also buffered by U43 and U44. Similarly, the output of U46 equals current through DUT divided by R20 value. Lock-in amplifier measures the voltage and current

complex phasor in a time division multiplexing fashion. The DUT impedance can be calculated using those two phasor and R20.

$$Z_{\mathrm{DUT}} = \frac{\mathrm{Voltage}}{\mathrm{Current}} R_{20} \qquad (6\text{-}1)$$

The accuracy of this circuit depends on the selection of U41, U42, U43, and U44, which must have low input capacitance, high input impedance as well as very high bandwidth. R20 behaves as a reference resistor in the system, thus R20 must have low temperature coefficient and very high precision rating. R20 is high precision thin film resistor. The system assumes the all operational amplifier are ideal, thus the working frequency of this circuit is limited to below 500 kHz.

6.3 Impedance Analyzer Test

The DUT is a standard 100 ohm resistor. The performance of this circuit will be compared with the Agilent 4294A precision impedance analyzer. The impedance measurement is repeated by 256 times for each system. The accuracy of those two impedance analyzers can be evaluated by the average output impedance and the precision can be learnt from output impedance standard deviation.

Figure 6.4 Device under test

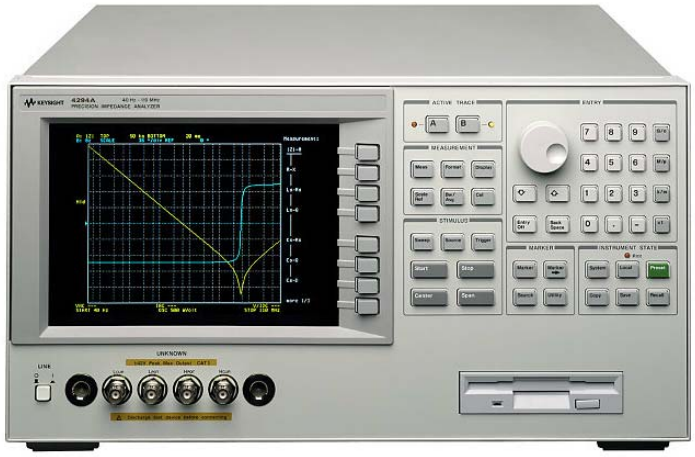


Figure 6.5 Agilent 4294A precision impedance analyzer

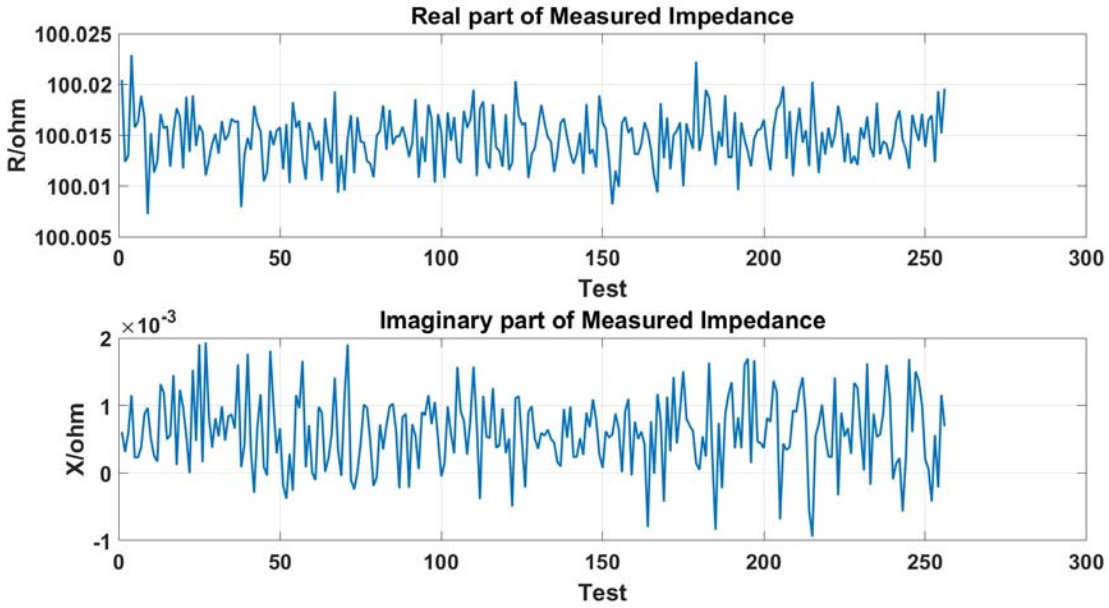
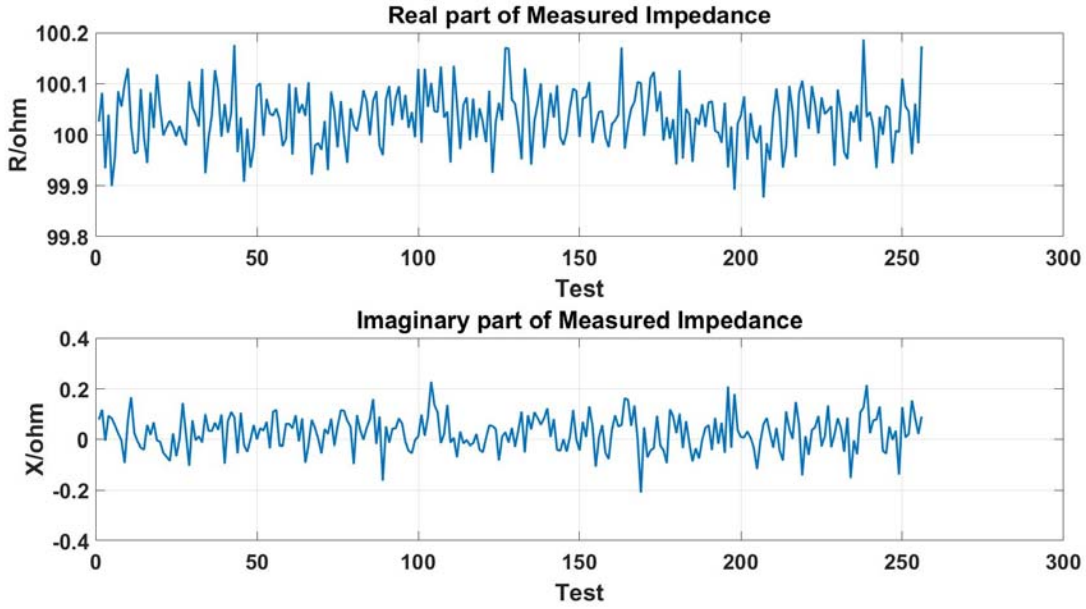
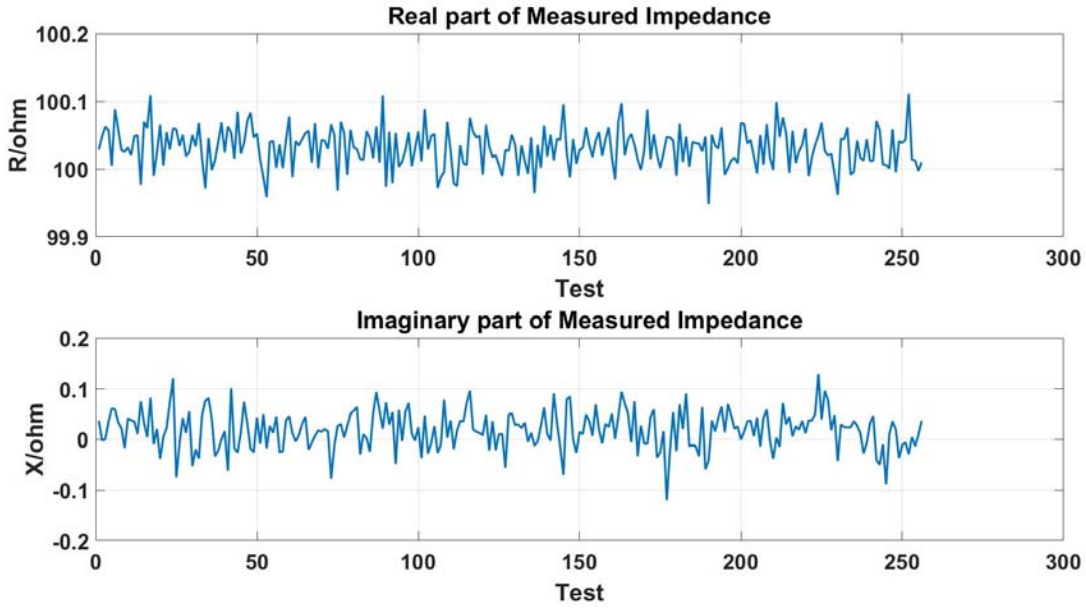


Figure 6.6 Impedance measured by the lock-in amplifier based impedance analyzer

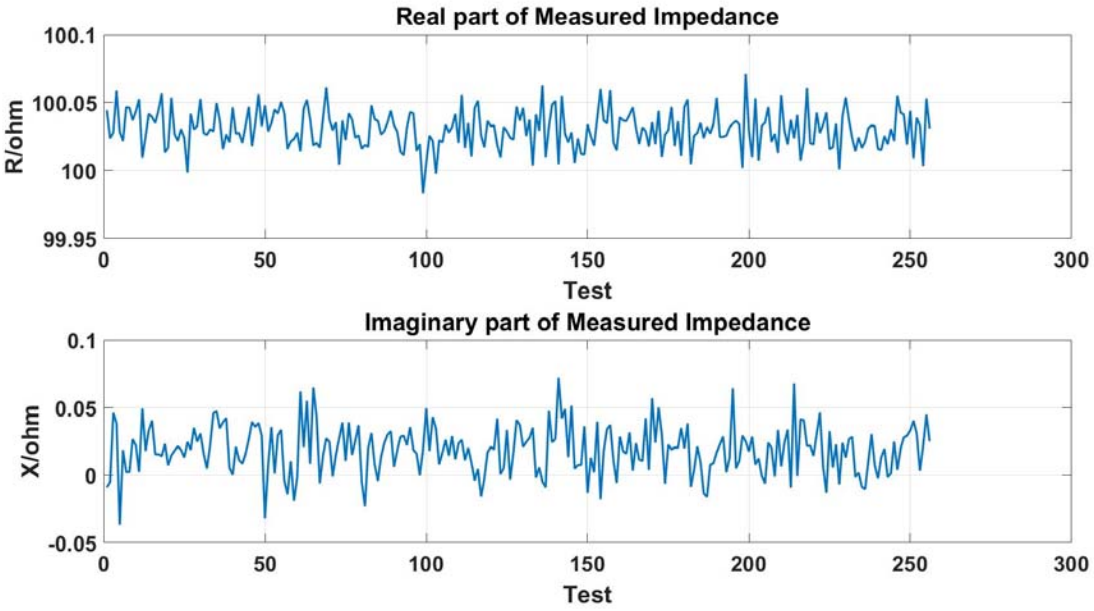


(a)

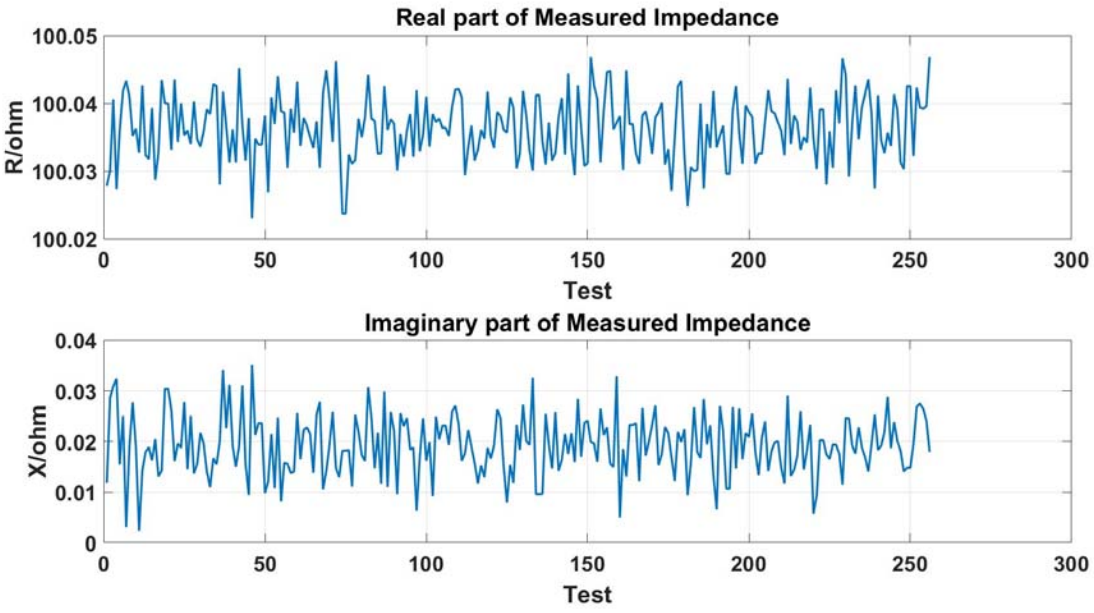


(b)

Figure 6.6 Impedance measured by this Agilent 4294A impedance analyzer (a) BW=1 (b) BW=2

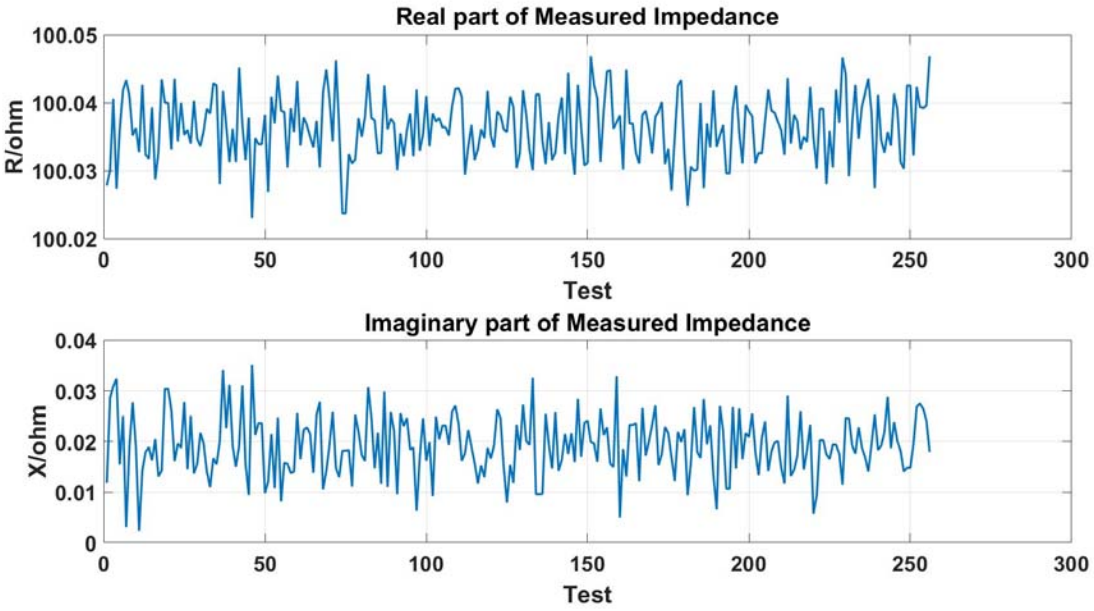


(c)



(d)

Figure 6.6(continued) (c) BW=3 (d) BW=4



(e)

Figure 6.6(continued) (e) BW=5. BW setting determines the noise level of Agilent 4294A, and BW=5 has the lowest noise.

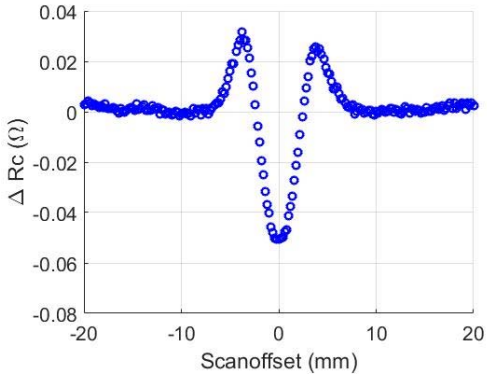
Table 6.1 Noise Performance Comparison

Configuration	Real Part Avg.	Real Part STD
Lock-in amplifier based impedance analyzer	100.015 Ω	2.61 mΩ
Agilent 4294A, BW=1	100.032 Ω	56.7 mΩ
Agilent 4294A, BW=2	100.032 Ω	29.5 mΩ
Agilent 4294A, BW=3	100.030 Ω	14.2 mΩ
Agilent 4294A, BW=4	100.035 Ω	10.0 mΩ
Agilent 4294A, BW=5	100.036 Ω	4.77 mΩ

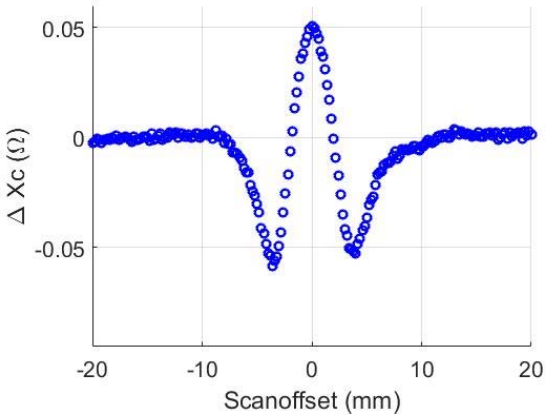
Table 6.1 illustrates that the proposed system is not only accurate but also has very high precision, and both performance specification exceed the best case from Agilent 4294A impedance analyzer.

6.4 Impedance Analyzer Application

The main application of this system is to obtain high quality data for small crack eddy current testing as shown in Figure 6.7. Please note the overall impedance change due to this crack is extremely small.

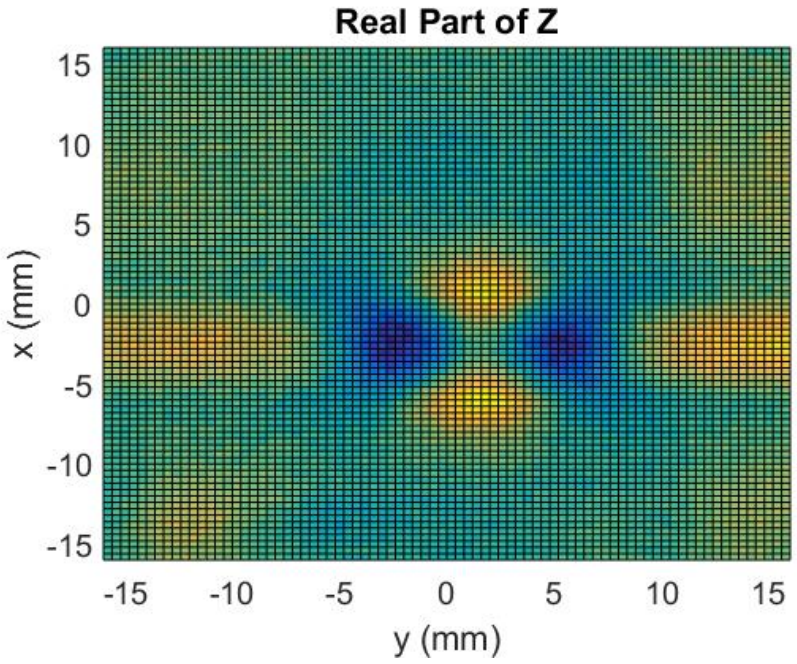


(a)

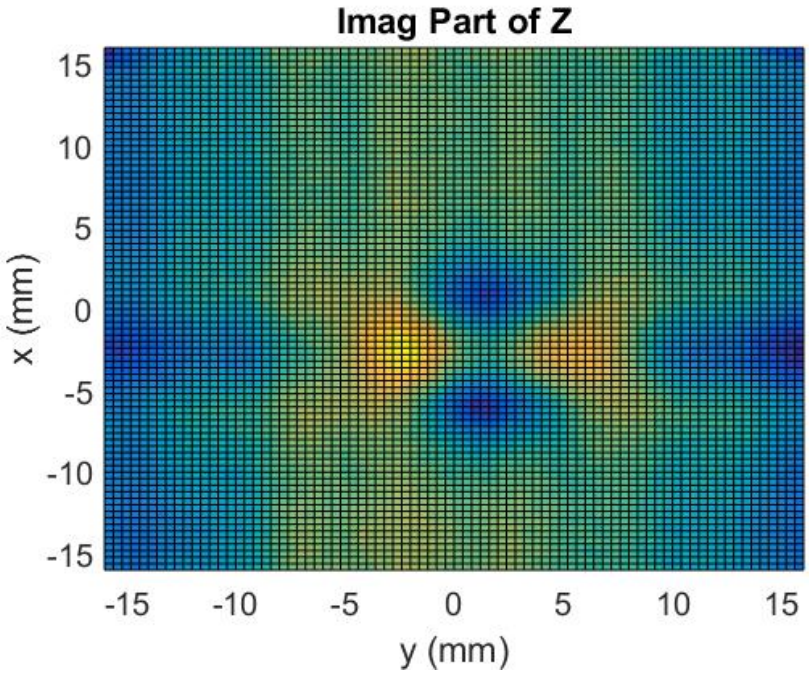


(b)

Figure 6.7 Small impedance change due to small surface crack (a) real part (b) imaginary part



(a)



(b)

Figure 6.7 2D scam for small impedance change due to small surface crack (a) real part (b) imaginary part

6.5 Conclusion

In this chapter, a simple but powerful impedance analyzer circuit is proposed. Combining this circuit and a lock-in amplifier, the system is able to provide high quality impedance data for frequencies below 500 kHz. The accuracy and precision of this system exceed those of a professional precision impedance analyzer.

CHAPTER 7. CONCLUSIONS AND FUTURE WORK

This thesis first gives introduction to potential drop method with emphasis on ACPD method. The well established theory and measurement system are discussed. Then the goal of this thesis is discussed because of the limitations of state-of-the-art system. Starting from chapter two, details in hardware design are given. High current, low noise DC-DC power converter supplies high quality power rails to the rest of the system. Fully programmable single tone and multi-tone direct digital synthesis sub-system ensures that system is able to generate any kind of excitation signal at the frequency of interest. Both high current and wide bandwidth transcondutance amplifiers make sure that the amplitude of drive current is desirable from 1 Hz to 100 kHz. Low noise continuous time low-pass filter cleans the raw pick-up signal before it reaches analog to digital converter for digitization. The ultra-low noise analog front end is designed with least amount of input referred noise possible. Because of the transconductance amplifier and low pass filter, the pick-up signal's SNR is greatly improved compared with legacy systems. Chapter three discusses system calibration as well as digital signal processing. The precision resistor based calibration scheme ensures the accuracy of this system, while the fast digital signal processing algorithm help to reduce data acquisition time significantly without sacrificing SNR. The fast digital signal processing algorithm use a much higher sampling frequency than conventional FFT method, thus the overall measurement speed can be improved. System speed test shows that for a 1 Hz to 100 kHz frequency scan, the time cost is 14.6 seconds, which is way faster than any other existing systems. The overall system SNR is higher than 64 dB from 1 Hz to 10 kHz, while the worst case SNR is 44 dB at 100 kHz. This ACPD system is also able to perform experiments in time domain. Transient potential drop measurements are performed on three finite thickness samples, and good agreement is observed between experiment results and numerical Laplace

inversion results. Because the conductivity and permeability in the numerical Laplace inversion are obtained from ACPD method on the same specimen, the transient potential drop measurements and alternating potential drop measurement have achieved consistency. This work also discovers that the overshoot of the transient potential drop response is linearly proportional to the permeability of the test specimen. This discovery can be used to quickly determine specimen's permeability. The last chapter discuss a lock-in amplifier based impedance analyzer for eddy current application. The noise of this impedance analyzer is lower than the state-of-the-art commercial impedance analyzer. This impedance analyzer makes the liquid metal eddy current test possible. In summary, this thesis discusses the design, test, verification and application of a ultra-fast ACPD standalone measurement system that is capable of time domain potential drop measurement. This system reduces a typical ACPD frequency scan from several hours to less than 20 seconds with better signal to noise ratio. This system greatly improves the productivity of ACPD method and has great potential for commercialization. Future work should focus on improve the thermal stability, reduce power consumption, reduce system complexity, upgrade USB communication and improve ACPD probe design.

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